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Design Strategies for Ultralow Power 10nm FinFETs

Abhijeet M. Walke
aw8188@rit.edu

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Design Strategies for Ultralow Power 10nm FinFETs

by

ABHIJEET M. WALKE

A Thesis Submitted in Partial Fulfillment of the
Requirements for the Degree of Master of Science in Electrical Engineering

Department of Electrical & Microelectronic Engineering

Kate Gleason College of Engineering

Rochester Institute of Technology

Rochester, NY

May 2017

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A Thesis Submitted in
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Electrical Engineering
Approved by:

| | |
|--|------|
| Dr. Santosh Kurinec Professor, (Thesis Advisor) | Date |
|--|------|

| | |
|---|------|
| Dr. Karl Hirschman Professor, (Committee Member) | Date |
|---|------|

| | |
|---|------|
| Dr. Robert Pearson Professor, (Committee Member) | Date |
|---|------|

| | |
|---|------|
| Dr. Garrett Schlenvogt Silvaco, Inc, (External Committee Member) | Date |
|---|------|

| | |
|---|------|
| Dr. Sohail Dianat Professor, (Department Head) | Date |
|---|------|

Department of Electrical and Microelectronic Engineering

R·I·T | **KATE GLEASON**
College of ENGINEERING

Rochester Institute of Technology
Rochester, New York

May, 2017

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Finally, I want to thank my parents and my elder brother for all the love and support that they gave me during this year. Without their support this thesis would not be here.

Dedicated to my parents

Abstract

Integrated circuits and microprocessor chips have become integral part of our everyday life to such an extent that it is difficult to imagine a system related to consumer electronics, health care, public transportation, household application without these small components. The heart of these circuits is, the metal oxide field-effect transistor (MOSFET) which is used as a switch. The dimensions of these transistors have been scaled from a few micrometers to few tens of nanometer to achieve higher performance, lower power consumption and low cost of production. According to the International Technology Roadmap for Semiconductors (ITRS), beyond 32 nm technology node, planer devices will not be able to fulfill the strict leakage requirement anymore due to overpowering short channel effects and need of multi-gate transistor is inevitable. The motivation of the thesis therefore is to investigate techniques to engineer threshold voltage of a tri-gate FinFET for low power and ultra-low power applications. The complexity of physics involved in 3D nano- devices encourages use of advanced simulation tools. Thus, Technology Computer Aided Design Tools (TCAD) are needed to perform device optimization and support device and process integration engineers. Below 20nm technology node, the Fin-shaped Field Effect Transistor or Tri-gate transistor requires extensive use of 3D TCAD simulations.

The multi-gate devices such as FinFETs are considered to be one of the most promising devices for Ultra Large Scale Integration (ULSI). This device structural design with additional gate electrodes and channel surfaces offers dynamic threshold voltage control. In addition, it can provide better short channel performance and reduced leakage. In this study, new design strategies for 10nm node NMOS bulk FinFET transistors are investigated to meet low power (LP) ($50\text{pA}/\mu\text{m} < I_{\text{OFF}} < 20\text{pA}/\mu\text{m}$) and ultralow power

(ULP) ($I_{\text{OFF}} < 20 \text{ pA}/\mu\text{m}$) requirements using three dimensional (3D) simulations. The punch-through stop implant dose (fin body doping), source\drain junction placement The and gate workfunction are varied in order to study the impact on the OFF state current (I_{OFF}), transconductance (g_m), gate capacitance (C_{gg}) and intrinsic frequency (f_T). It is shown that the smallest gate length device can meet the requirements of LP transistors and ULP transistors by engineering of source-drain extension engineering, fin body doping concentration and choice of gate workfunction.

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List of Symbols

| Symbol | Unit | Description |
|-----------------|-------------------|--|
| λ_N | cm | Natural length of transistor with ‘N’ no. of gates |
| ϵ_{Si} | F/cm ² | Dielectric constant for silicon |
| ϵ_{ox} | F/cm ² | Dielectric constant for gate dielectric |
| t_{ox} | cm | Thickness of gate dielectric |
| t_{Si} | cm | Thickness of Si body |
| SS | mV/dec | Subthreshold Swing |
| $DIBL$ | mV/V | Drain Induced Barrier Lowering |
| V_{GS} | V | Gate to source voltage |
| V_{DS} | V | Drain to source voltage |
| ψ_S | V | Surface Potential |
| C_{ox} | F/cm ² | Gate oxide capacitance |
| I_{OFF} | A | OFF state current |
| I_{DS} | A | Drain to source current |
| I_{ON} | A | On state current |
| E_g | eV | Bandgap |
| V_T | V | Threshold voltage |
| K | J/K | Boltzma’s Constant |
| T | K | Temperature |
| q | C | Unit charge |
| n_i | cm ⁻³ | Intrinsic carrier concentration |
| W | nm | Width of the transistor |
| L_G | nm | Gate length of transistor |
| g_m | A/ μ V | Transconductance |
| f_T | Hz | Transit frequency |

Abbreviations

| | |
|--------|--|
| 2D | Two Dimensional |
| 3D | Three Dimensional |
| BOX | Buried Oxide |
| BTBT | Band-to-Band Tunneling |
| CMOS | Complementary Metal Oxide Semiconductor |
| CVD | Chemical Vapor Deposition |
| DIBL | Drain Induced Barrier Lowering |
| EOT | Effective Oxide Thickness |
| FET | Field Effect Transistor |
| FinFET | Fin based 3D Field Effect Transistor |
| GAA | Gate All Around |
| GIDL | Gate Induced Drain Leakage |
| IC | Integrated Circuits |
| ITRS | International Technology Roadmap for Semiconductor |
| MOS | Metal oxide Semiconductor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NMOS | N-channel MOSFET |
| PMOS | P-channel MOSFET |
| SCE | Short Channel Effect |
| TCAD | Technology Computer Aided Design |
| TEM | Transmission Electron Microscopy |

Chapter 1

Introduction

In the early 20th century, advent of vacuum tube began the era of electronics industry. Soon after that solid state switches were invented as a solution to the problems associated with vacuum tubes. In 1960, the first metal oxide semiconductor field-effect transistor based on Si/SiO₂ system was demonstrated by D. Kahng and M. Atalla [1]. Since then, continuous efforts are being made to scale the geometry of transistors and improve their packaging density while keeping the fabrication cost low. This geometry scaling not only reduced chip cost per transistor but also improved the chip operating frequencies. It was estimated that with the rigorous dimensions scaling, the static power (device is in OFF state) would become higher than actual active power (device is in ON state) density. This made the device designer to change the scaling approach. Gordon Moore in 1965 predicted (Fig. 1.1) exponential growth of number transistors in integrated circuits(IC). Today there are billions of transistors found in a single IC [2]. Over the course of few years after 1990s, MOSFETs have undergone various changes to improve performance while maintaining side effects associated with scaling as low as possible. At one point, the geometry scaling became responsible for sub threshold degradation, which will be discussed in following sections.

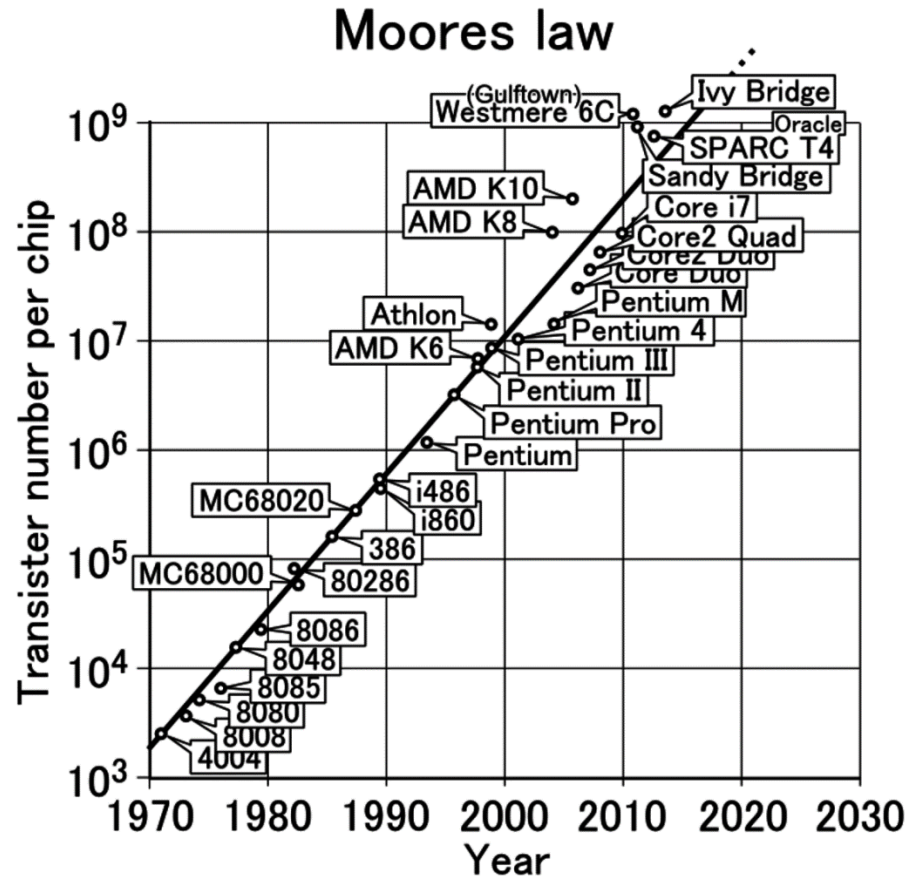


Figure 1.1 Transistor count as a function of year showing the doubling of transistor count every two years [3].

1.1 Limitations of the Planar MOSFET

The main motivation behind the scaling of device geometry is to improve its performance, reduce the device area and lower power consumption. Over the decades, the device dimensions have been scaled from few 10 micrometer to below 10s of nanometer. In 1974 Robert H. Dennard introduced a set of rules for scaling long channel transistors in order to avoid detrimental effects on device characteristics and to continue Moore's law [4]-[5]. The transistors scaling involves scaling of channel length, source/drain junction depth, channel width, gate oxide thickness, channel doping concentration, transistor pitch, interconnect and power

supply to maintain device reliability and electrostatic integrity. In the following subsection the challenges associated with scaling are briefly discussed

1.2 Short Channel Effects

As the dimensions of transistors are shrunk, the channel length becomes same order of magnitude as the source and the drain depletion layer width. Close proximity between the source and channel reduces gate control and causes undesirable effects called as “Short Channel Effect” (SCE). These effects include drain induced barrier lowering (DIBL) where drain bias can modulate the drain current [6]. Punch-through occurs when the channel doping is very low and short gate results in merging of source-channel and drain-channel junctions. Threshold voltage roll off is defined as the decrease in threshold voltage of MOSFET with decrease in gate length. Hot carrier degradation which can be responsible for reduction in lifetime of MOSFET. Gate leakage consist of direct and Fowler-Norheim and trap assisted tunneling through gate oxide layer. Gate induced drain leakage (GIDL) which is band-to-band tunneling mechanism occurs at the highly doped drain and gate overlap region. Short channel effects mainly result in increase in OFF state current, degradation of ON current and weak gate electrostatics.

Today’s planar MOSFETs feature high-k dielectric with metal gate has led substantially reduction gate leakage and mobility improvement by means of source/drain stressor and silicidation of source and drain (Fig.1.2) [7]. In spite of many technological challenges, planar MOSFET shows poor subthreshold swing ($>80\text{mV}/\text{dec}$) and much higher OFF current ($>100\text{nA}/\mu\text{m}$) when gate length is

scaled below 30nm. Therefore, further scaling of planar bulk MOSFET is becoming more and more challenging.

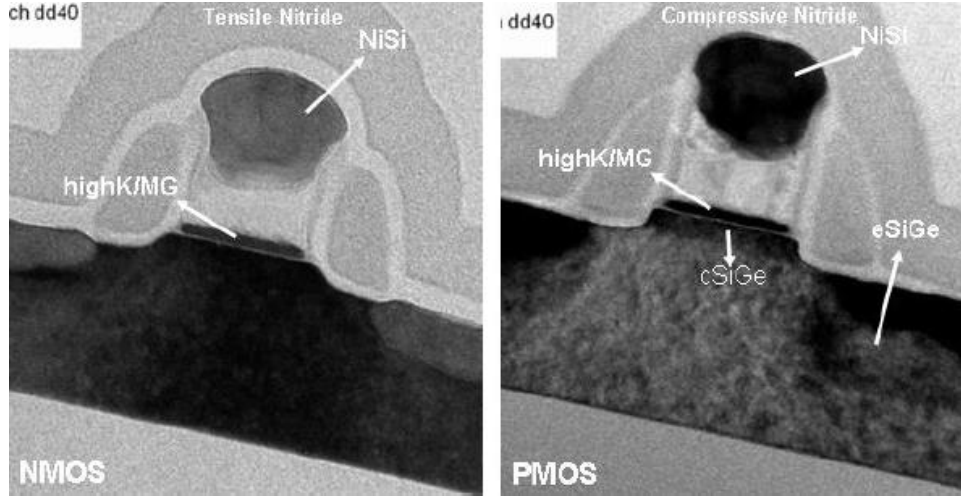


Figure 1.2 Transmission Electron Microscopic Images of NMOS and PMOS devices showing high-k metal gate stack. NMOS shows tensile nitride stress layer and PMOS shows compressive stress layers, channel and source/drain SiGe epitaxial layer [7].

One way to minimize these short channel effects is to improve gate electrostatics. This can be achieved by increasing the number of gates and reducing body thickness.

1.3 Multigate Transistor

The natural/characteristics length of transistor is a measure of electrostatic control of channel [8]. It represents the penetration distance of electric field lines from the drain to the channel of body or the amount of control drain has over the channel since both gate and drain compete for that control. [9]. For multigate device, natural length is given by,

$$\lambda_N = \sqrt{\frac{\epsilon_{Si}}{N\epsilon_{ox}}} t_{ox} t_{Si} \quad (1.1)$$

Where N is the effective number of gates, ϵ_{Si} is the permittivity of silicon, ϵ_{ox} is the permittivity of gate oxide, t_{ox} is thickness of gate oxide and t_{Si} is thickness of silicon. From equation (1.1), it is possible to predict the silicon body thickness required to minimize the short channel effect. If λ is greater than 5 to 6 times the gate length, device is considered to be relatively free of short channel effect.

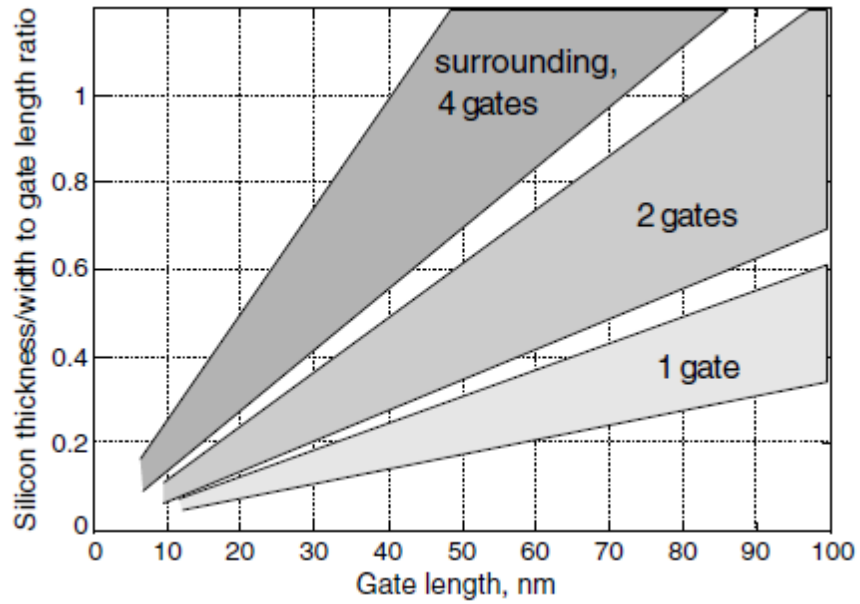


Figure 1.3 Maximum allowed silicon film thickness and device width versus gate length [9].

Fig. 1.3 shows the ratio of the maximum allowed silicon film thickness and device width versus gate length to avoid the short channel effects. The film thickness requirements for triple-gate, Pi-gate and omega-gate devices are located between those for double-gate and surrounding-gate devices. It reveals that, for the gate length of 20 nm the thickness of silicon film in triple gate device needs to be less than half of the gate length. As per the prediction made by ITRS, multigate transistors such as FinFETs will be necessary to

mitigate short channel effect and to enable further scaling of transistors. Fig.1.4 shows different FinFET architecture that can be used for technology nodes 22 nm and beyond [10].

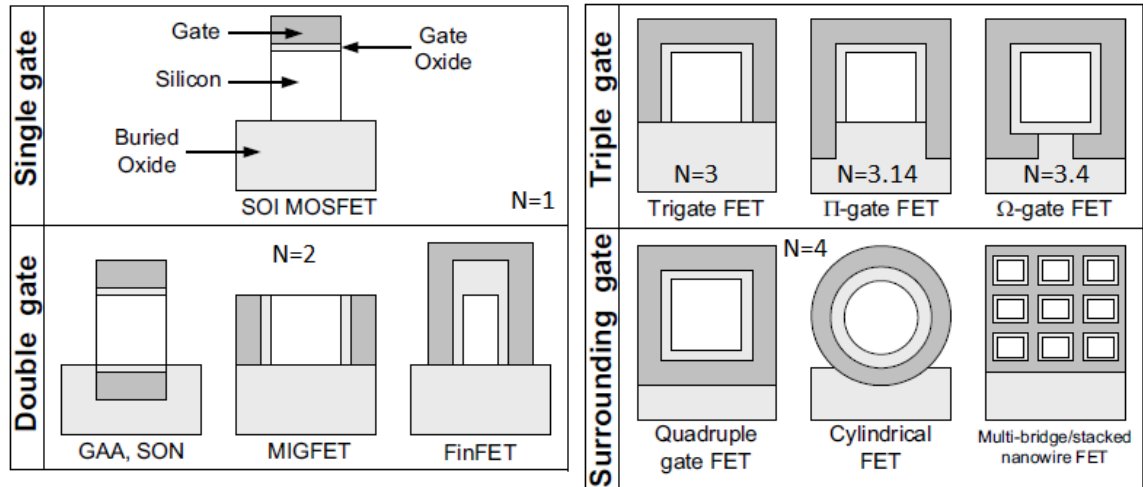


Figure 1.4 Various multigate architectures with effective number of gates [10].

1.4 History of FinFETs

In 1989, a first DEpleted Lean-channel TrAnsistor (DELTA) was fabricated successfully [11]. To eliminate the issues related to device scaling, two different device structures were proposed. The first theory was to make effective device length longer than depletion layer width by using vertical MOSFETs. The second method was to use thin film technology, such as Separation by Implanted Oxygen (SIMOX) to shrink the device thickness smaller than the depletion-layer width. The Fig. 1.5(a) shows a schematic cross section of device. The distinctive feature of DELTA was formation of a bulk single crystal using selective oxidation which offers high-quality single Si crystal [11]. DELTA gate controls channel potential from both sides more effectively which results in better device

characteristics as compared to the conventional devices. For the planar MOSFET, band bends only on the one side where as DELTA gate can control the channel from both side.

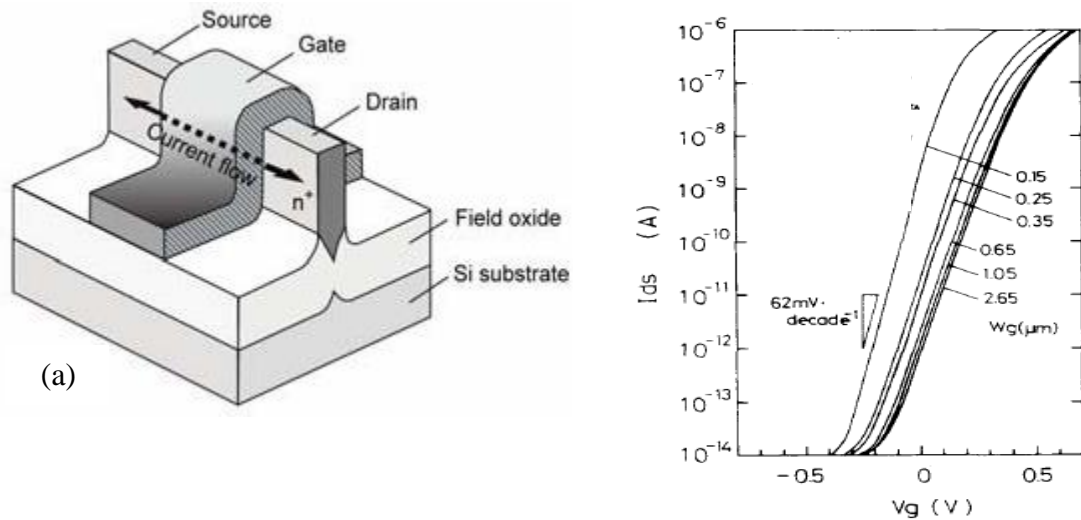


Figure 1.5 (a) Schematic cross section of DELTA and (b) Subthreshold characteristics as a function of channel thickness (W_g) [11]

The subthreshold swing is also small since the width of the thin Si channel (W_g) corresponds to substrate thickness. Experimental results show that a decrease in W_g less than $0.3 \mu\text{m}$ results in small subthreshold swing. Due to large effective width, ON current of DELTA is greater than that of planar MOSFET.

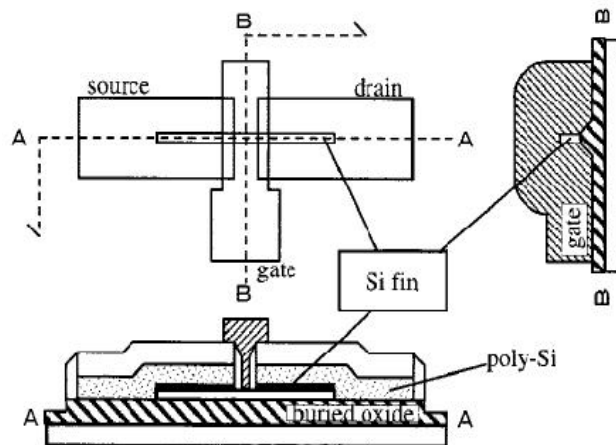
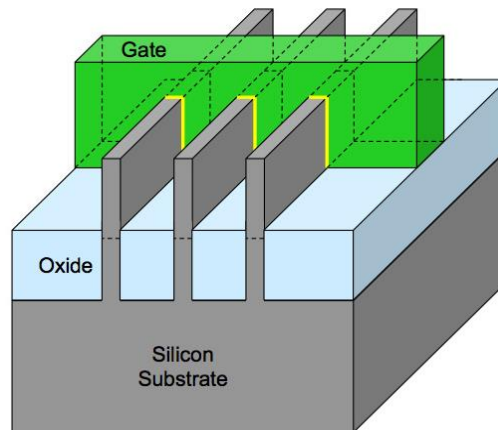
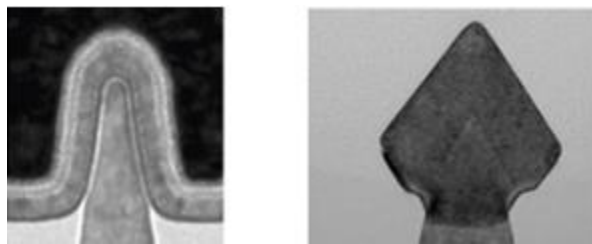


Figure 1.6 FinFET layout and schematic cross sectional structure [12].

Fig. 1.6 shows the layout and schematic of a self-aligned double gate MOSFET, FinFET. A "vertical" surface of Si-fin acts as channel and current flows parallel to the wafer surface [12]. Poly-Si film is heavily doped and wrapped around Si-fin. Further simplified FinFET processes were developed [13], which enabled FinFET scaling and improved drive current for future devices obtained by different gate workfunction engineering and thinner gate oxide. In 2011, Intel Corporation announced a new transistor technology called “3D Tri-gate”



(a)



(b)

Figure 1.7 (a) FinFET Structure. (b) TEM images of intel 22nm tri-gate transistor [14]

Figure 1.7(a) displays the structure of a tri-gate FinFET. The gate wraps around the channel “Fin” to provide better gate control. The taper fin structure with rounded corner can

be seen in transmission electron microscopic image taken across the gate and source/drain epi to reduce parasitic resistance, strain improvement as shown in Fig. 1.7(b). Gate induced drain leakage (GIDL) is found to be the limiting factor in achieving ultralow values ($<100\text{pA}/\mu\text{m}$) of OFF current. There are several studies which discuss approaches to reduce GIDL [15][16]. The I_{OFF} can be lowered by increasing the threshold voltage of the transistor. This can be achieved by multi-threshold voltage techniques such as changing WF [17],[18] engineering SD extension region and by increasing length of the gate. Longer gate length enables lower leakage and mitigates short channel effects (SCEs) for LP and ULP transistors [19]. However, it tends to degrade analog figure of merit (FOM) such as cut-off frequency, $f_T = gm/2\pi C_{gg}$ where C_{gg} is the total gate capacitance [19]. This is because gm decreases and C_{gg} increases with increase in the gate length.

Different techniques have been proposed such as HALO implant, graded channel design to overcome the degradation of figure of merit [20]. However, in nanoscale devices, enabling these techniques poses technological challenges. The concept of gate-source/drain overlap/underlap engineering has been studied to overcome short channel effects (SCEs) and lowering OFF current [21]-[22].

1.5 Need for Low Power Devices

The internet of things (IoT) is becoming an increasingly growing topic of conversation for the past couple of years. The basic concept of IoT is connecting any device to the Internet. This includes everything from cellphones, coffee makers, washing machines, wearable devices and almost anything else we can think of. According to the prediction made by Cisco and Erricson company, there will be over 50 billion connected devices by 2020.

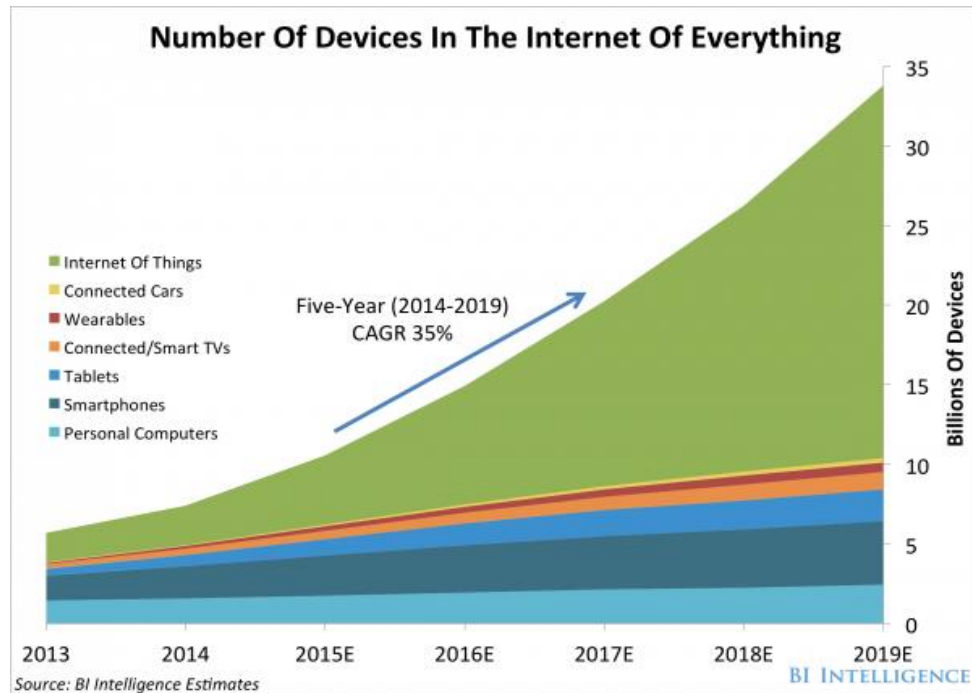


Figure 1.8 IoT market expansion through 2019 [23].

The graph shows a progress of personal devices such as mobile phones, personal computers, laptops, tablets. However, this growth is restricted by number of people on the planet. The real growth is from all these devices connected to each other in areas like home automation, hospitals, transportation. Virtually there will be unlimited devices. All these devices should consume less power and must have long battery life but also should not compromise in performance.

The device characteristics of transistor families are summarized in Table. 1.1 for 22nm technology node. A high-speed transistor logic family is categorized into two device type- High Performance (HP) and Standard Performance (SP). These transistor families have gate length of 30-32nm and subthreshold leakage ranging from 100nA/ μm to 1nA/ μm . A low standby power product requires low leakage (<50pA/ μm) with

subthreshold slope of $< 65\text{mV/dec}$ and DIBL of 30mV/V . This can be achieved by increasing the gate length or junction engineering optimizations.

Table 1.1 Transistor Logic family classification for NMOS FinFET

| Transistor Type | High Speed Logic | | Low Power Logic | |
|---|-----------------------|---------------------------|----------------------|-----------------------|
| Option | High Performance (HP) | Standard Performance (SP) | Low Power (LP) | Ultra Low Power (ULP) |
| V_{DD} (V) | 0.75 | 0.75 | 0.75 | 0.75 |
| L_{gate} (nm) | 30 | 34 | 34 | 40 |
| I_{Dsats} @0.75V (mA/ μm) | 1.08 | 0.71 | 0.41 | 0.35 |
| I_{OFF} | 100 nA/ μm | 1 nA/ μm | 30 pA/ μm | 15 pA/ μm |

The total power dissipation of the CMOS circuit is given by

$$P_{Total} = \underbrace{f_{clk} \alpha C V_{DD}^2}_{\text{Dynamic}} + \underbrace{V_{DD} I_{leakage}}_{\text{Static}} \quad (1.2)$$

Where f_{clk} is the clock frequency, α is the average switching activity, C is the total capacitance, V_{DD} is the supply voltage and $I_{leakage}$ is the leakage current. The dynamic power is proportional to square of the supply voltage and clock frequency. In addition, leakage current has also exponential dependence on supply voltage. Thus, lowering the supply voltage will be effective way to reduce dynamic power. However, scaling of supply voltage requires to lower the threshold voltage. Since the leakage current depends exponentially

on threshold voltage, the leakage current increases considerably and therefore there is need to develop strategy to reduce leakage current which effectively reduces static power. At scaled technology node possible architectures are planer Fully Depleted Silicon on Insulator (FD SOI), and FinFET. However, FD SOI has higher wafer cost and suffers from self-heating effect. Thus, FinFET is considered for 22nm technology node and beyond.

Chapter 2

Theory of FinFET

Multi-gate MOSFET has been considered to be a replacement over conventional planar MOSFETs. In Double-gate MOSFETs (DGFET), a second gate is added opposite to the traditional gate as shown in Fig. 2.1 which gives better control over SCEs.

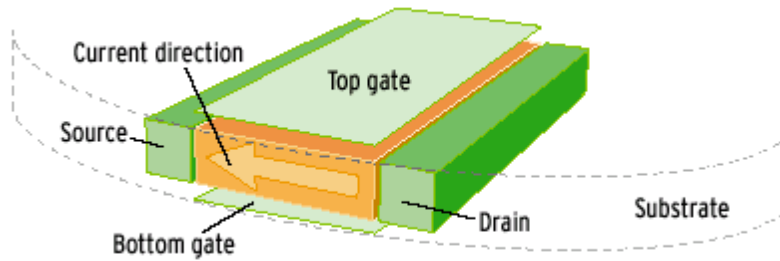


Figure 2.1 Double gate MOSFET with top and the bottom gate [24].

The common mode of operation is to switch both gates simultaneously. Due to the second gate in DGFETs, the longitudinal electric field produced by the drain is blocked from the source end of the channel. This results in reduced drain induced-barrier lowering (DIBL) and better sub-threshold swing. The process of perfectly self-aligned double gates fabrication has been difficult in DGFETs. To overcome this issue, fin-type double/triple gate MOSFET was studied in 1989. FinFET is a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor where the gate wraps around the thin conducting channel called “Fin”. Fig 2.2(a) shows the basic 3D structure of tri-gate FinFET. Since the channels is completely covered by the gate, the overall inversion layer is larger as seen in Fig. 2.2(b), which results more drain current. It can be improved with multiple fins. This structure also allows very little leakage current flow through the body when the transistor is in OFF state and therefore results in better performance and low static power.

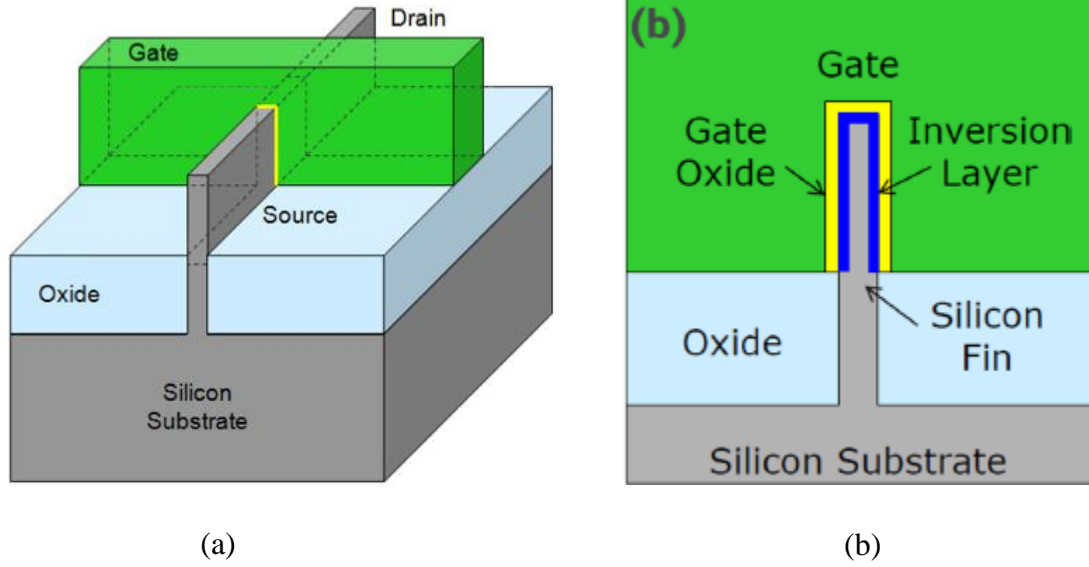


Figure 2.2 (a) 3D tri-gate FinFET Structure. (b) Cross section along the Fin [25].

The electrical width of tri-gate FinFET is $W = 2H_{fin} + T_{fin}$. Where H_{fin} is height of fin and T_{fin} is thickness of fin. The operation of FinFET is largely similar to double gate FET. In Double gate FET the top gate is ineffective (due to thicker gate dielectric) as a result $W = 2H_{fin}$.

2.1 Double-gate MOSFET (DGFET)

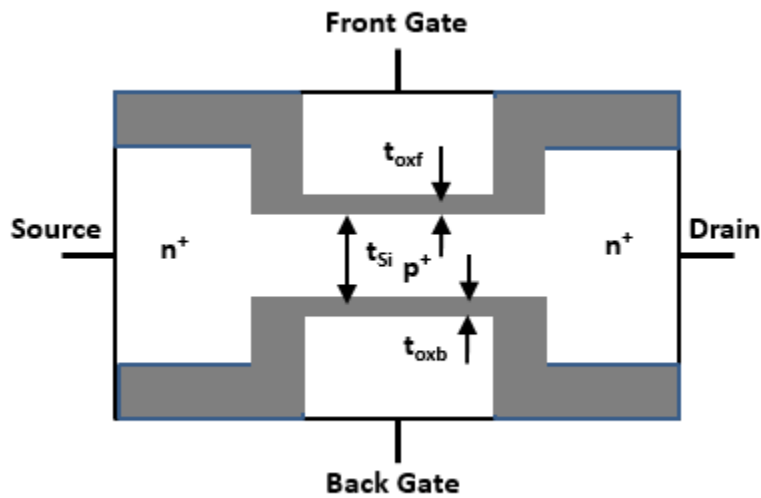


Figure 2.3 Schematic of n-channel DGFET

In Fig. 2.3, gate dielectric is shown by shaded grey region. The parameters t_{oxf} and t_{oxb} represent the front and back gate dielectric. The front and back gate controls the channel. This helps in reducing the encroachment of drain electric field into channel and therefore leads to reduced short channel effects. There are basically two types of DGFETs. A symmetric DGFET has similar material and gate dielectric thickness for both front and back gate electrode wherein asymmetric DGFETs the two gate electrode has different workfunction.

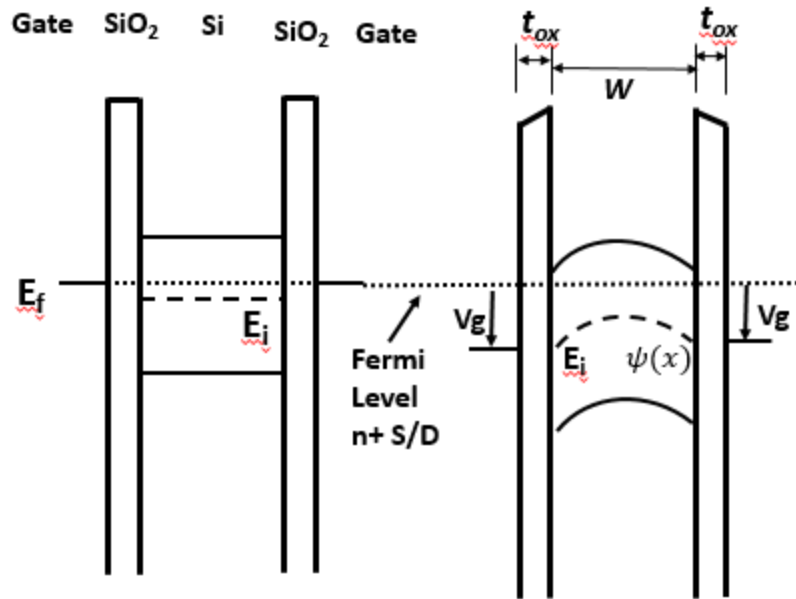


Figure 2.4 Energy band diagram of symmetric DGFET (a) $V_g = 0V$ (b) $V_g = V_t$

Energy band diagram for symmetric DGFET is shown in Fig. 2.4 for different bias conditions. At zero gate bias, the bands remain flat as long as silicon is lightly doped and depletion charge is negligible. When gate bias is increased, the bands in silicon bends

downwards near quasi fermi level which increases the carrier density near the sidewall and the device is strongly inverted.

1.5.2 Analytical Drain-Current Model for Double-gate MOSFET

A continuous analytical current-voltage model for DG MOSFET is developed by Yaun Tauer et al [26]. It uses closed solution of Poisson's equation and current continuity equation without charge sheet approximation. The schematic of undoped symmetric MOSFET is shown in Fig. 2.5

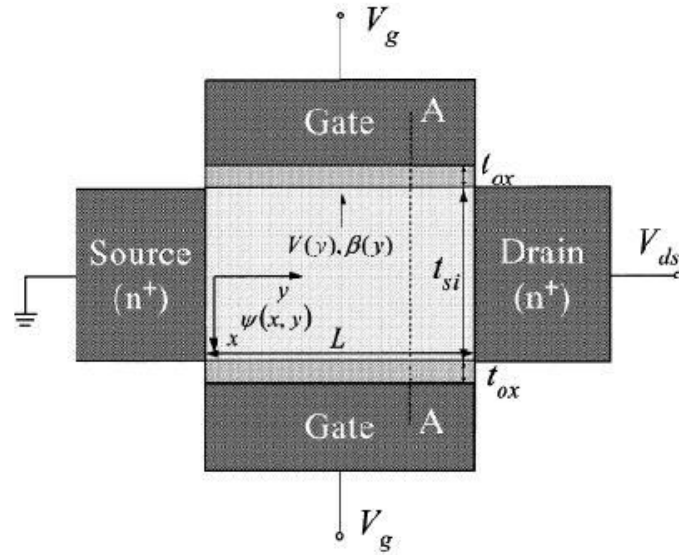


Figure 2.5 Schematic diagram of DG MOSFET.

$V(y)$ is the quasi-fermi potential at the point in the channel and β is the function of V .

Poisson's equation along the vertical cut perpendicular to silicon film results following expression

$$\frac{d^2\Psi}{dx^2} = \frac{q}{\epsilon_{si}} n_i e^{\frac{q(\Psi-V)}{kT}} \quad (1.5.1)$$

The gradient of quasi-fermi level potential is in the direction of current flow along the y direction. Solution of equation (1.5.1) is

$$\Psi(x) = V - \frac{2kT}{q} \ln \left[\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\epsilon_{si} kT}} \cos \left(\frac{2\beta x}{t_{si}} \right) \right] \quad (1.5.2)$$

Where β is constant which can be determined by the boundary conditions. Drain current in linear and saturation region is given by

$$I_{DS} = 2\mu C_{ox} \frac{W}{L} \left(V_g - V_t - \frac{V_{DS}}{2} \right) V_{DS} \quad (1.5.3)$$

$$I_{DS} = 2\mu C_{ox} \frac{W}{L} \left[\left(V_g - V_t \right)^2 - \frac{8rk^2T^2}{q^2} e^{\frac{q(V_g - V_0 - V_{DS})}{kT}} \right] \left(V_g - V_t - \frac{V_{DS}}{2} \right) V_{DS} \quad (1.5.4)$$

Where

$$V_t = V_0 + \delta, \quad V_0 = \Delta\phi + (2kT/q) \left\{ \ln \left[(2/t_{si}) \left(\sqrt{2\epsilon_{si} kT / q^2 n_i} \right) \right] \right\}, \quad (1.5.5)$$

$\delta = (2kT/q) \ln [q(V_g - V_0)/4rkT]$, $r = \epsilon_{si}t_{ox}/\epsilon_{ox}t_{si}$ is structural parameter and $\Delta\phi$ is a workfunction of top and bottom gate electrodes with respect to the intrinsic semiconductor.

2.2 Bulk FinFET fabrication process flow

The fabrication of FinFET begins with the formation of fin. The conventional lithography used to form fin is shown in Fig. 2.6. In this approach, a stacked layers of Si_3N_4 and SiO_2 hard mask are deposited via chemical vapor deposition [28] as shown in Fig 2.6(b). Fin etch is followed by an oxide fill step for isolation purpose [Fig. 2.6(d-f)]. The oxide deposition must fill deep and should be voids or defect free. Next step is to etch back the oxide to the silicon fin height [Fig. 2.6(h)]. A high dose angle implant at the bottom of fin serves as punch-through stop layer and completes the isolation. After fin fabrication, the FinFET fabrication process is similar to the standard MOSFET process flow consisting of source and drain implant followed by gate stack deposition.

Advanced technology node FinFET technology uses Self Align Double Patterning (SADP). The process is depicted in Fig. 2.7. The process begins sacrificial layer or dummy gate deposition and patterned shown in Fig. 2.7 (a). A layer of hard mask made of SiO_2 or Si_3N_4 is deposited using CVD as shown in Fig. 2.7(b). The spacers are formed (Fig. 2.7(c)) by etching back the oxide back. The final step is to remove sacrificial layer creating fins as shown in Fig.2.7(d). Advantage of using spacer lithography technique is multiple fin pitches can be implemented using a single lithography step. The main manufacturing challenges for bulk FinFETs are controlling the etch along the edges to generate uniform fin widths and vertical edges.

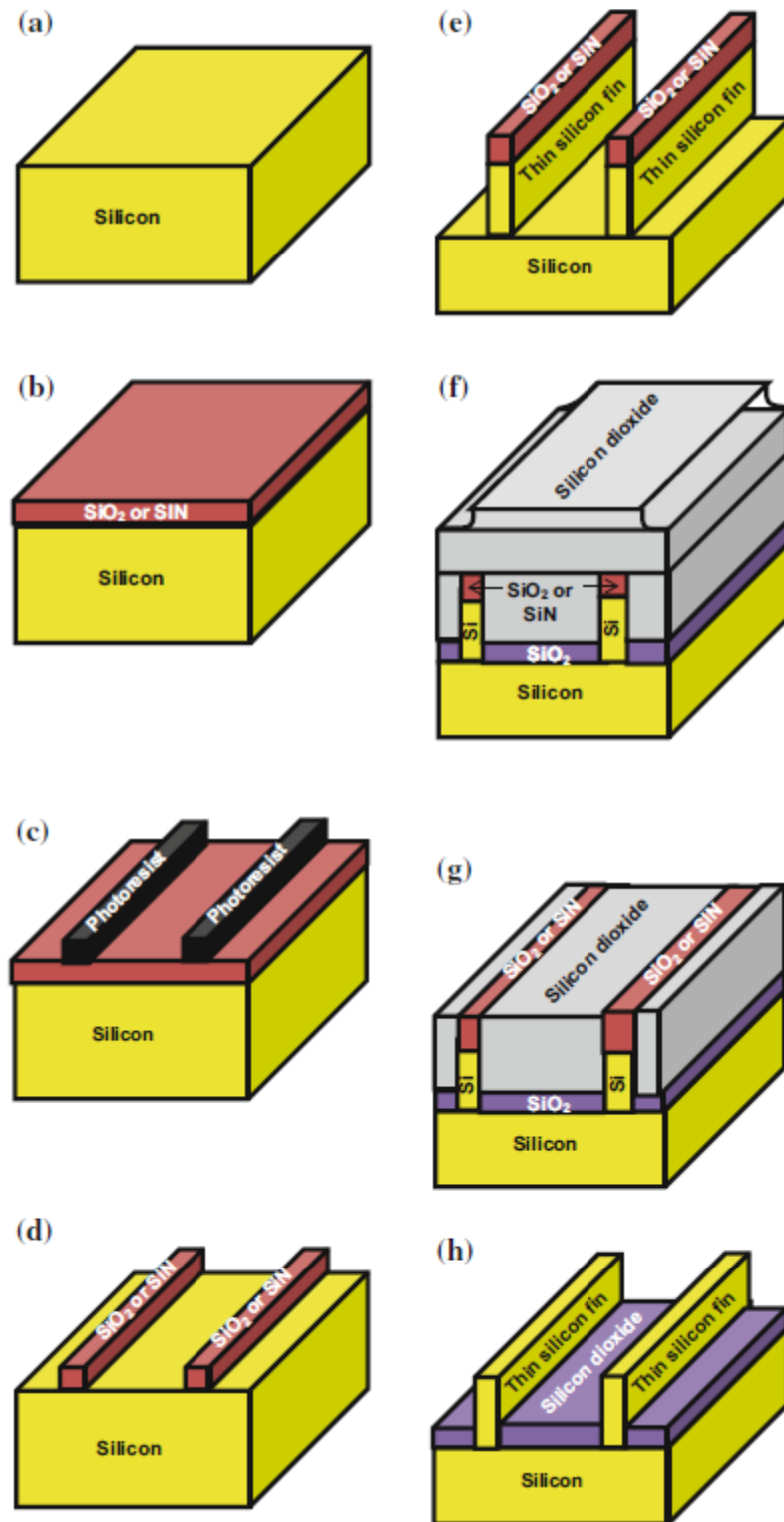


Figure 2.6 Conventional bulk FinFET process flow [27].

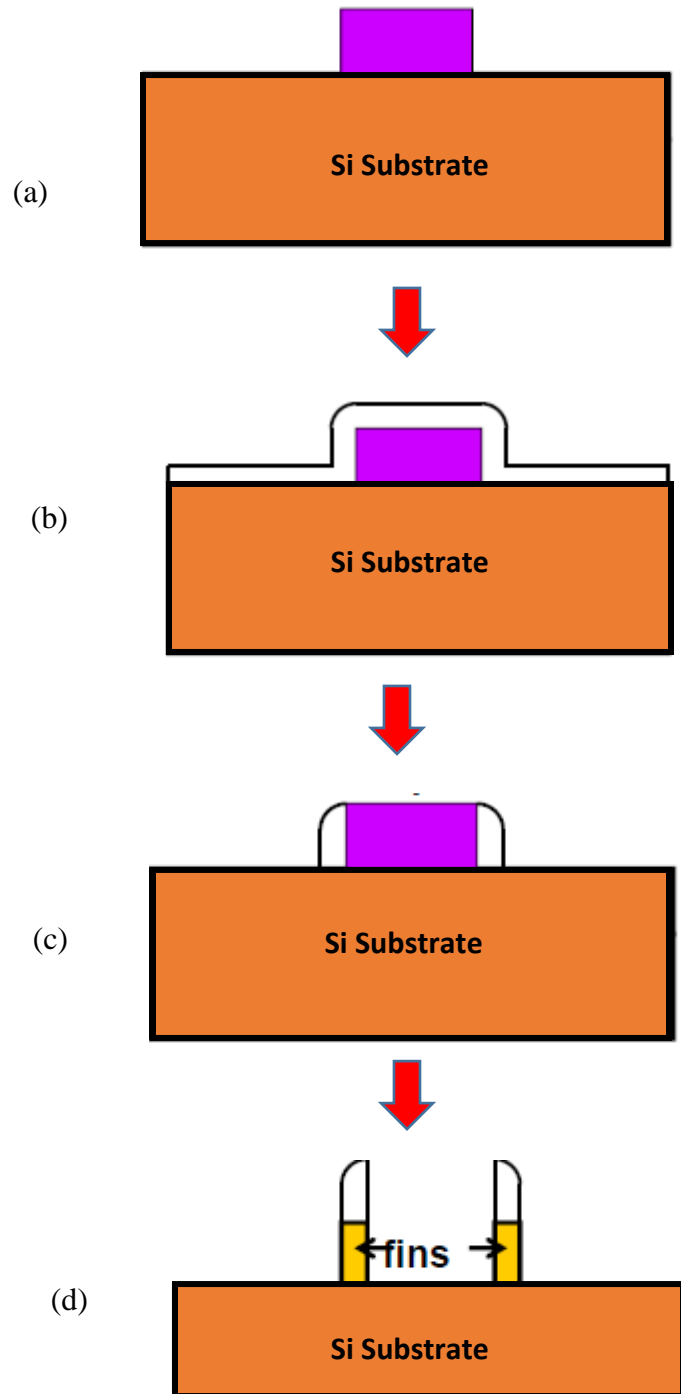


Figure 2.7 Self-Align Double Patterning process flow [29].

2.3 Thesis Organization

This thesis is focused on understanding of the FinFET architecture and various threshold voltage techniques for low and ultra-power applications through 3D TCAD process and device simulation using Silvaco. The contents of thesis are organized into four major chapters followed by conclusion and future work. Chapter-1 begins with the limitation of planer MOSFETs and the need for low power devices for future technology node.

Chapter-2 presents the history of FinFET followed by literature review. The principal operation of multigate transistor is discussed by explaining physics of double gate MOSFET. Comparison between the conventional and SADP fin fabrication flow is also discussed. Chapter-3 describes the simulation methodology for 20nm gate length FinFET and discusses about the models used for device simulation. Models are calibrated by comparing simulated current-voltage characteristics with experimental results.

In Chapter-4, effect of fin geometry with quantum confinement effect on ON and OFF-state current is studied. This is followed by effect of various threshold voltage techniques such as punch-through doping, source/drain extension engineering and workfunction on transconductance and OFF current discussed in chapter 5.

Chapter-6 draws main conclusion of thesis and suggestion for further work are offered.

Chapter 3

Simulation Methodology

Three-dimensional process and device simulations of tri-gate FinFETs were performed using Silvaco 3D Victory Process and Victory Device [30] process and device simulators. FinFETs are created using deposition, etching, diffusion, and Monte-Carlo implantation modules of VictoryProcess. The device structure created in VictoryProcess is imported to VictoryDevice to perform electrical simulations.

3.1 Device Construction

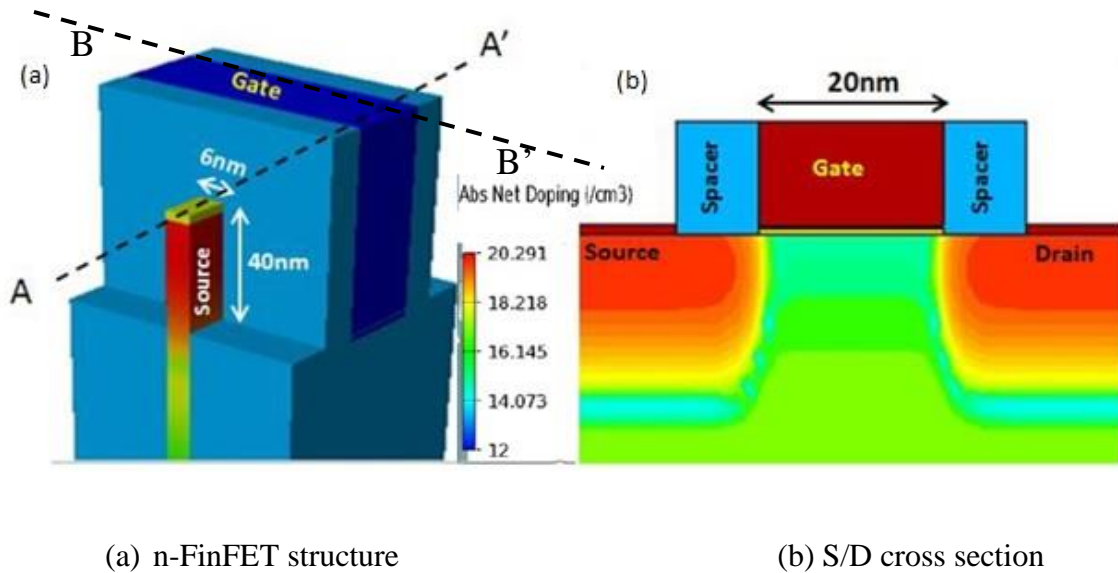


Figure 3.1 (a) n-FinFET 3D structure (b) source/drain cross section along AA' labeled in logarithmic scale

Table 3.1 Parameters used for simulated FinFET

| Parameters | Value |
|-----------------------------|--------------------------------------|
| Gate length | 20 nm |
| Fin height (H_{fin}) | 40 nm |
| Fin thickness (W_{fin}) | 6 nm |
| Gate oxide thickness (EOT) | 0.83 nm |
| Source/Drain doping | $1.5 \times 10^{20} \text{ cm}^{-3}$ |

A nominal gate length was chosen to be 20nm with rectangular fin height of 40nm and width of 6nm. A double gate insulator of $\text{HfO}_2/\text{SiO}_2$ (0.19nm/0.5nm) resulting in an equivalent oxide thickness of 0.83nm was adopted in the simulation as summarized in table 3.1. Effective oxide thickness (EOT) indicates how thick SiO_2 film would need to produce same gate capacitance as high-k material. EOT is defined as

$$EOT = t_{high-k} \left(\frac{k_{SiO_2}}{k_{high-k}} \right) + t_{SiO_2} \quad (3.1.1)$$

Where t_{high-k} is thickness of HfO_2 = 1.9nm, k_{SiO_2} and k_{high-k} is dielectric constant for SiO_2 and HfO_2 respectively and t_{SiO_2} is thickness of interfacial SiO_2 which is 0.5 nm. Therefore, EOT is 0.83nm. Fig.3.1 shows the device constructed using Victory Process. The source drain doping of $1 \times 10^{20} \text{ cm}^{-3}$ and fin doping of $1 \times 10^{16} \text{ cm}^{-3}$ is used. A channel stop implant has been created with a doping ranging from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$. For punch-through doping, angle implant is used in order to have lightly doped channel (top of fin) as shown in Fig. 3

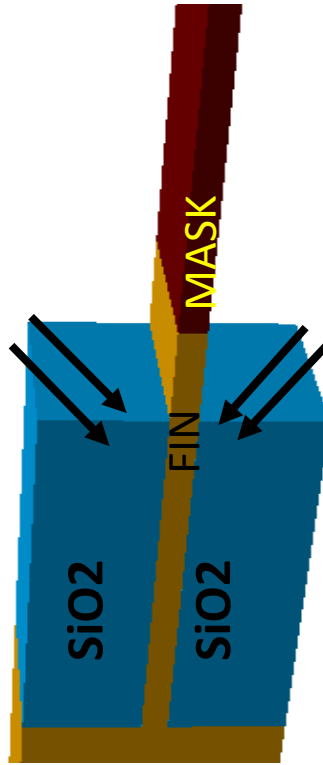


Figure 3.2 Illustration of angle implant for punch trough doping shown by arrows

3.2 Device Simulation

The device simulations employed use the Bohm Quantum Potential (BQP) model to take into account quantum confinement of carries in three dimensions [31]. The mobility in the surface channel is modeled using the 'CVT' model that takes into account the effects of transverse and longitudinal fields [32]. Other effects such as Auger and concentration dependent Shockley-Read-Hall recombination is also included in simulations. Hurkx model with its band-to-band tunneling (BTBT) formulation has been incorporated to analyze GIDL [33]. Each model will be discussed briefly.

3.2.1 Auger recombination

Auger recombination involves three-particle transition where mobile carrier either emitted or captured. When an electron and recombines, energy is transferred to the third electron in conduction band which then thermalizes back down to conduction band edge. Auger recombination modeled using following expression [34]

$$R_{Auger} = C_n n(np - n_{ie}^2) + C_p p(np - n_{ie}^2) \quad (3.1)$$

Where n and p is the electron and hole concentration respectively and n_{ie} is the effective intrinsic concentration. The coefficients C_n and C_p are constant. For this work, we have used standard auger recombination model.

3.2.2 Shockley–Read–Hall Recombination (SRH)

Shockley-Read-Hall recombination is also called as recombination through defects. It is a two step process.

- Electron or hole is trapped by an energy levels present in forbidden gap due to defects in crystals.
- If the hole goes up to the same energy level before electron is thermally excited to the conduction band, then it recombination occurs.

The SRH recombination rate is given by [35],

$$R_{SRH} = \frac{np - n_{ie}^2}{\tau_p \left[n + n_{ie} \exp\left(+\frac{ETRAP}{kT_L}\right) \right] + \tau_n \left[p + n_{ie} \exp\left(-\frac{ETRAP}{kT_L}\right) \right]} \quad (3.2)$$

Where τ_p and τ_n are the electron and hole life times, n and p are the electron and hole concentrations, n_{ie} is the effective intrinsic concentration and T_L is the lattice temperature. $ETRAP$ is the difference between the trap energy level and the intrinsic fermi level. The concentration dependent SRH lifetime model calculates carrier lifetime as a function of the impurity concentration.

3.2.3 Lombardi CVT mobility model

The Lombardi models used in this work is combined model that accounts for low field and transverse field effect on mobility. It also combines doping, temperature and inversion layer effect. The electron and hole mobilities are expressed as

$$\frac{1}{\mu_n} = \frac{1}{\mu_{n0}} + \frac{f_n}{\mu_{n,ac}} + \frac{f_n}{\mu_{n,sr}} \quad (3.3)$$

and

$$\frac{1}{\mu_p} = \frac{1}{\mu_{p0}} + \frac{f_p}{\mu_{p,ac}} + \frac{f_p}{\mu_{p,sr}} \quad (3.4)$$

The first components on the right-hand side of the expression represents low field bulk mobility limited by intervalley phonon scattering. The second term represents surface mobility limited by acoustic phonons scattering and the third component is surface roughness factor.

3.2.4 Band to Band Tunneling

Gate induced drain leakage is the most important leakage mechanism which need to reduce to achieve low OFF current. The mechanism responsible for GIDL is band to

band tunneling (BTBT) which occurs near gate-drain overlap region. Fig. 3.3 shows the band diagram representation near gate-drain overlap region under high electric field.

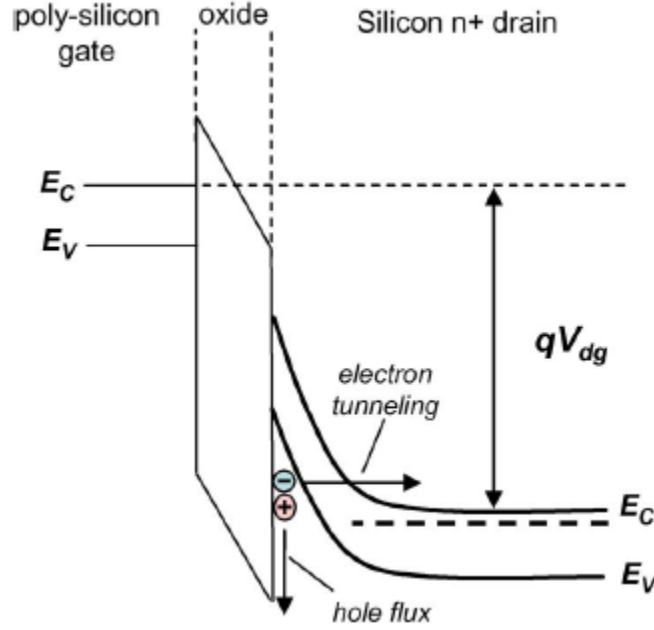


Figure 3.3. Energy band diagram showing BTBT generation.

When the drain of NMOS is connected to supply voltage, lowering the gate bias results in high electric field. The depletion region is formed between the drain and gate overlap region. When the electric field is sufficiently high enough to cause band bending larger than band gap of silicon, the BTBT process is initiated. The electron in the valance band can tunnel through the conduction band. The electron in the conduction band is collected by the drain terminal and hole is swept to body terminal thus creating GIDL current flowing from drain contact to body.

For analysis of GIDL current, standard Hurkx BTBT model is used. The BTBT generation is given by following expression [33]

$$G_{BTBT} = A. \exp\left(\frac{-B}{E}\right) \cdot \left(\frac{E}{E_1}\right)^P \quad (3.5)$$

Where $E_1 = 1 \text{ V/cm}$; $P=2$ and 2.5 for direct and indirect transition BTBT respectively; A and B are Kane's parameters given by

$$A = \left(\frac{q^2}{h^2}\right) \left(\frac{2}{E_G}\right)^{\frac{1}{2}} (m_0 \text{ MASS.TUNNEL})^{\frac{1}{2}} \quad (3.6)$$

and

$$B = 2\pi^2 \left(\frac{1}{qh}\right) \left(\frac{E_G}{2}\right)^{\frac{3}{2}} (m_0 \text{ MASS.TUNNEL})^{\frac{1}{2}} \quad (3.7)$$

Where q is the unit electron charge, h is Plank's constant, E_G is the band gap and m_0 is the mass of electron. The *MASS.TUNNEL* is the relative mass for tunneling. For indirect transition (silicon), A is $4 \times 10^{14} \text{ cm}^{-3} \text{ s}^{-1}$ and B is $1.9 \times 10^7 \text{ V/cm}$.

3.2.5 Bohm Quantum Potential model

The Bohm quantum potential (BQP) model incorporates quantum confinement effect in the drift-diffusion and energy balance equation. It is used to model quantum confinement effect in MOSFET channels and heterojunction semiconductor. BQP is defined for each single particle eigenfunction. An equation for an effective quantum potential for each carrier type is solved rather than solving Schrodinger equation directly. To calculate the density and transport of carriers, the quantum potential is added to the electrostatic potential.

The potentials are defined at each node by simultaneously solving a transcendental equation. The equation for electron is given by [30]

$$q\phi_{BQ,n} = E_{BQ,n} = -BQP.NGAMMA \left(\frac{\hbar^2}{2m_0}\right) \frac{\nabla (M^{-1} \nabla_n^{BQP.NALPHA})}{n^{BQP.NALPHA}} \quad (3.8)$$

and equation for hole is

$$q\phi_{BQ,p} = E_{BQ,p} = -BQP.NGAMMA \left(\frac{\hbar^2}{2m_0} \right) \frac{\nabla (M^{-1} \nabla_n^{BQP.PALPHA}}{n^{BQP.PALPHA}} \quad (3.9)$$

Here $\phi_{BQ,n}$ and $\phi_{BQ,p}$ is the Bohm quantum potential for electron and holes. $E_{BQ,n}$ and $E_{BQ,p}$ is the energy equivalent to the Bohm quantum potential for electrons and holes. M^{-1} is the inverse effective mass. For n-type bulk FinFET the BQP for electron (bqp.n) is chosen with $bqp.ngamma = 1.3$ and $bqp.nalpha = 0.3$.

The simulated results are compared in Fig. 3.4 with recently reported experimental results of 20nm gate length nFinFET [36], validating the models used.

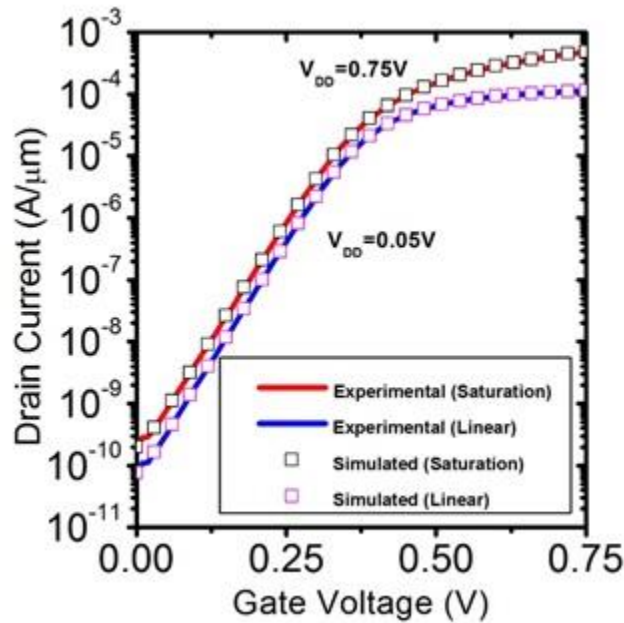


Figure 3.4 Comparison of experimental and simulated I_{DS} - V_{GS} characteristics of a 20nm nFinFET.

3.3 Definition of I_{ON} , I_{OFF} and V_T

In this work, ON-state current is defined at gate voltage (V_{GS}) of 0.75V and operating voltage (V_{DD}) of 0.75V as depicted in Fig. 3.5. The drain current I_D is normalized to total width of FinFET which is defines as $W_{eff} = 2 \times H_{fin} + T_{fin}$.

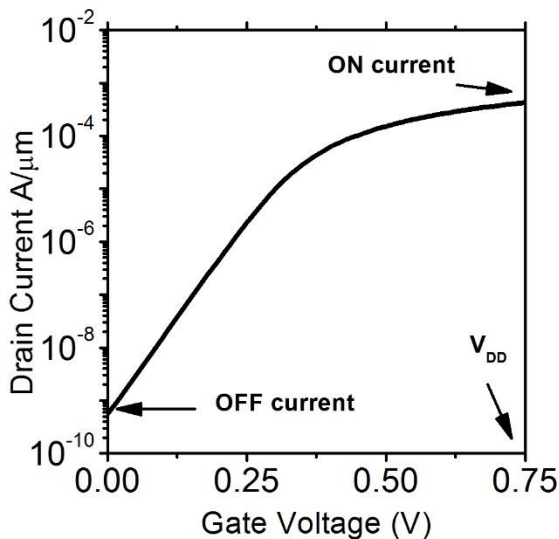


Figure 3.5 Transistor current-voltage characteristics.

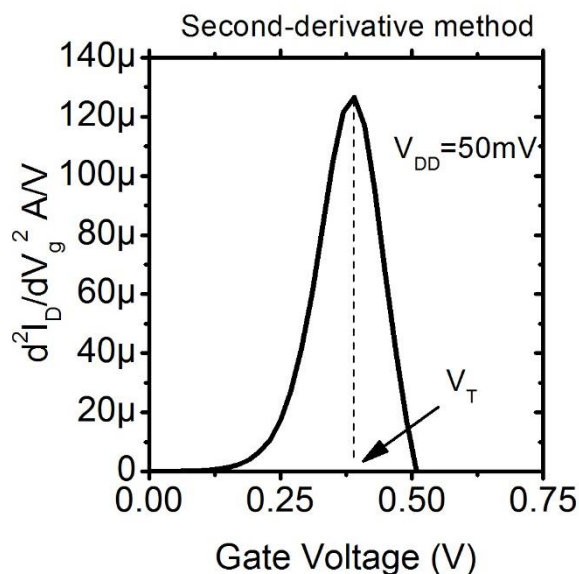


Figure 3.6 SD method showing plot of d^2I_D/dV_g^2 versus V_{GS} at $V_{DD} = 50\text{mV}$.

There are several methods of threshold voltage extraction from the measured drain current versus gate voltage transfer characteristics. In this work, threshold voltage is extracted using second-derivative (SD) of transconductance extrapolation method in linear region. It determines V_T as gate voltage at which derivative of transconductance (i.e. $dg_m/dV_{GS} = d^2I_D/dV_g^2$) is maximum. DIBL is extracted using $DIBL = (V_{th,sat} - V_{th,lin}) / (V_{DS,sat} - V_{DS,lin})$. Where $V_{th,sat}$ and $V_{th,lin}$ are the threshold voltage values at saturation and linear mode respectively. $V_{DS,sat}$ is 0.75V and $V_{DS,lin}$ is 0.05V.

Chapter 4

Effect of Fin Geometry

In chapter 1, different SCEs were studied which makes difficult for scaling of planar MOSFETs. To minimize the effect of drain electric field in the channel, planar MOSFETs rely on 1) scaling of gate oxide and 2) higher channel doping. The use of thinner gate oxide results in direct gate tunneling current whereas higher channel doping concentration reduces channel mobility and increase in GIDL current. In this section, we will discuss the effect of fin height and fin thickness on subthreshold characteristic of bulk FinFET.

4.1 Effect of Fin Height

As it was discussed in previous sections, the effective width of FinFET depends on fin height ($W_{eff} \propto 2H_{fin}$). Therefore, ON current can be improved by increasing fin height. Typically, FinFET has two to four fins in the same structure to boost ON current.

Fig. 4.1 shows ON and OFF state current at 0.75V drain bias. There is 33% increase in ON current when fin height is increased from 26nm to 40nm. Taller fin creates channel with larger effective volume resulting in higher ON current. OFF state current is not changed significantly as long as punch-through stop doping is sufficient enough to suppress SCEs. The subthreshold swing, DIBL and threshold voltage remains unchanged with increasing fin height as seen in Fig. 4.2. Thus, taller fins are preferred to exhibit more drive current per unit area.

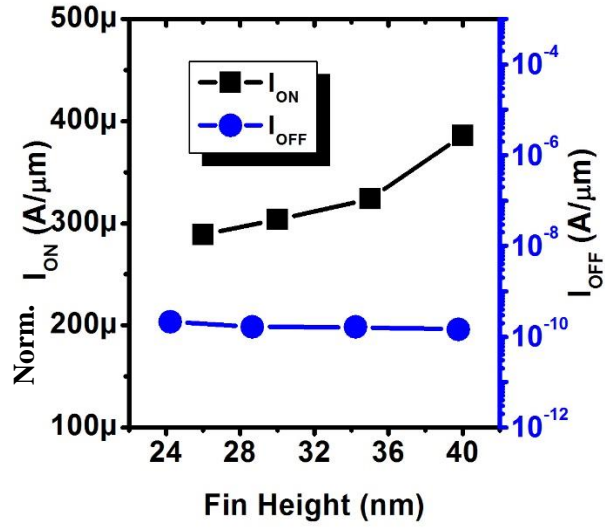


Figure 4.1 Plot showing ON and OFF state current for different fin height.

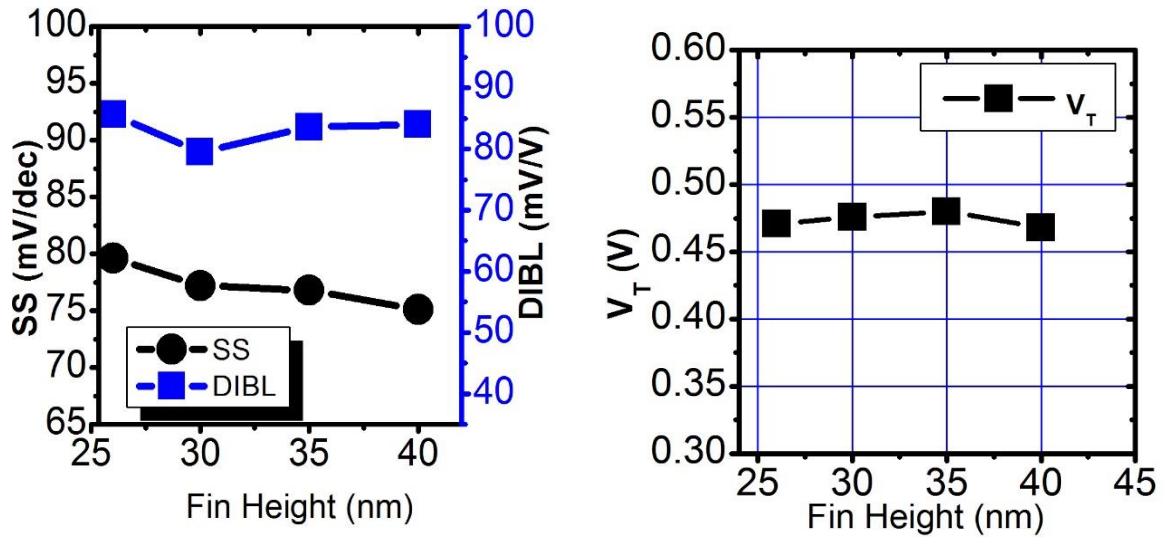


Figure 4.2 (a) Fin height versus DIBL and SS (b) Threshold voltage variation with fin height.

4.2 Effect of Fin Thickness

In multi-gate devices fin thickness plays important role in reducing Short channel effects. As it was introduced in chapter 1, the natural length, λ represents a measure of

SCE. To minimize the SCE, smaller value of λ is desirable. As it can be seen in equation 1.1, λ is proportional to square root of body thickness and gate oxide thickness. Thus, there is always a trade off t_{ox} scaling with fin thickness reduction.

Effect of fin thickness was studied on 20nm gate length FinFET. Fig. 4.3 shows I_D - V_G characteristics for fin thickness of 6nm, 8nm, 12nm and 14nm. It can be seen from the Fig 4.3(a) that, ON current increases with fin thickness. This is due to increase in channel volume inversion and effective fin width of FinFET. Fig. 4.3(b) presents short channel effects on OFF state current. Fin thickness of 6nm shows much lower OFF current than 14nm. As the fin becomes thicker, DIBL and SS degrade which increase leakage current. Fig. 4.4(a) shows linear increase in DIBL and SS. For the thick silicon film, drain electric field penetration into channel is more. Thus, gate loses control over channel and DIBL increases. The degradation of SS is due to poor gate control over channel region with increased in channel volume.

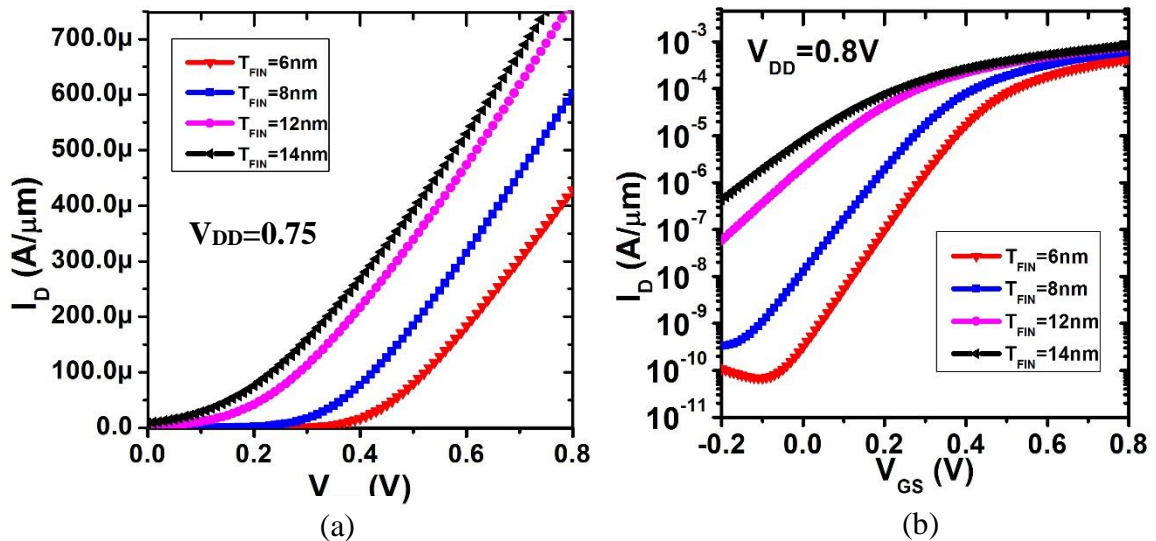


Figure 4.3 I_D - V_G comparison for different fin height (a) Linear I_D (b) Log I_D

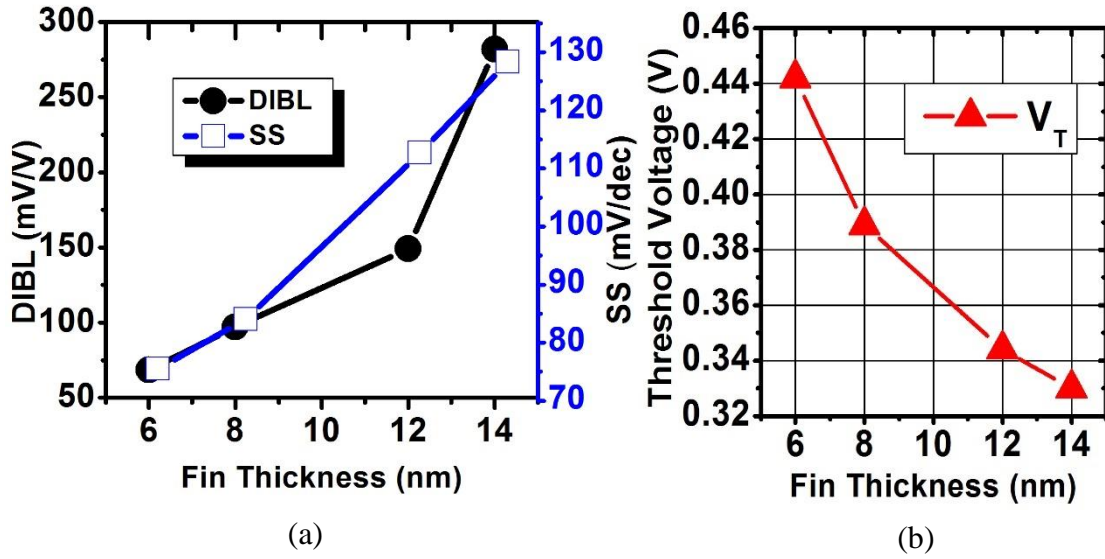


Figure 4.4 (a) Fin height versus DIBL and SS (b) Threshold voltage variation with fin height.

Fig. 4.4(b) shows variation of threshold voltage with fin thickness. Threshold voltage reduces with increase in fin thickness. For shorter channel length, the surface potential depends on the capacitance of source-fin and drain-fin junction rather than just capacitive coupling between the gate and channel. As the thickness of fin increases, the width of source-fin and drain-fin depletion region increases, which reduces the source-fin and drain-fin capacitance, thus coupling between the gate and surface potential increases [9]. And hence the threshold voltage decreases with increase in fin thickness. When fin thickness is reduced below 10nm, the quantum confinement (QC) effect becomes more significant. Quantum confinement creates strong sub-band energy splitting, causing reduced density of states and increase threshold voltage. Fig. 4.5 shows comparison of the electron current density perpendicular to channel for 16nm and 6nm fin thickness.

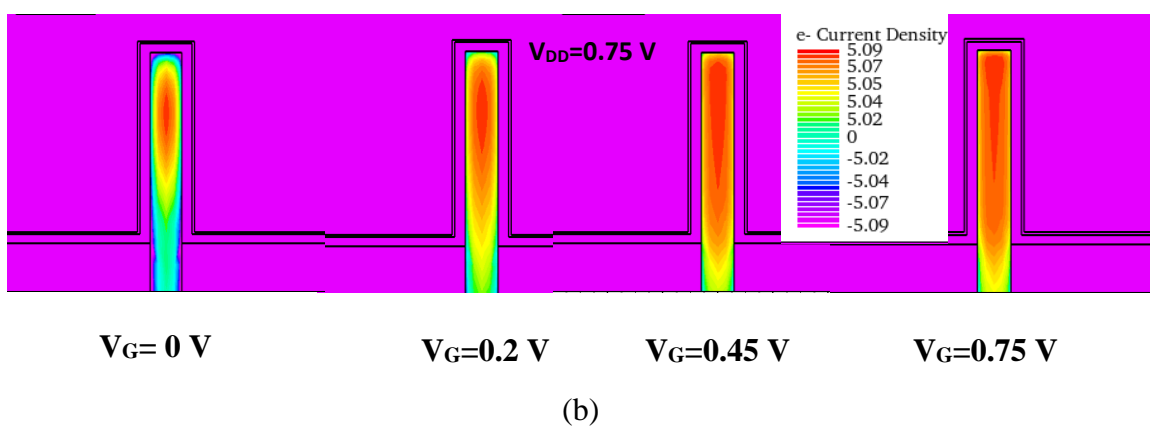
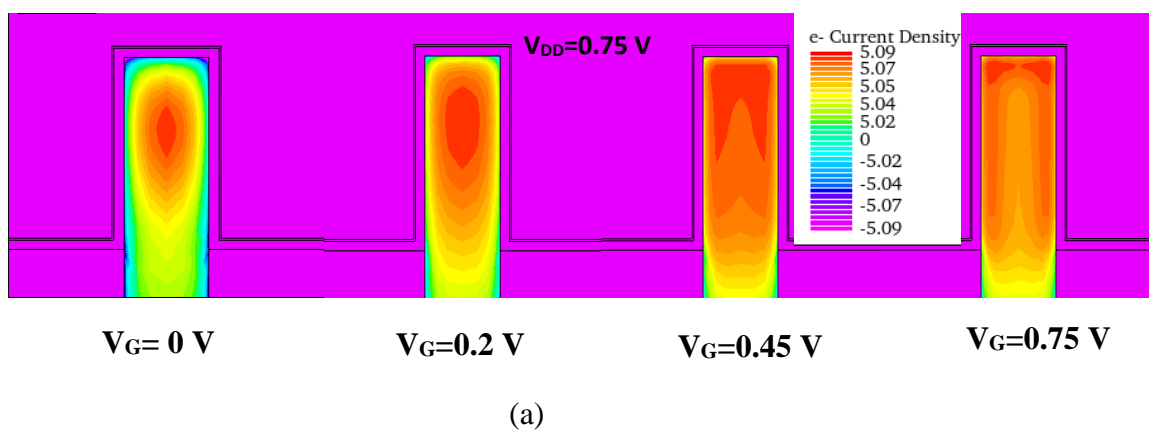


Figure 4.5 Electron current density perpendicular to channel (BB') labeled in logarithmic scale (a) 16 nm (b) 6 nm

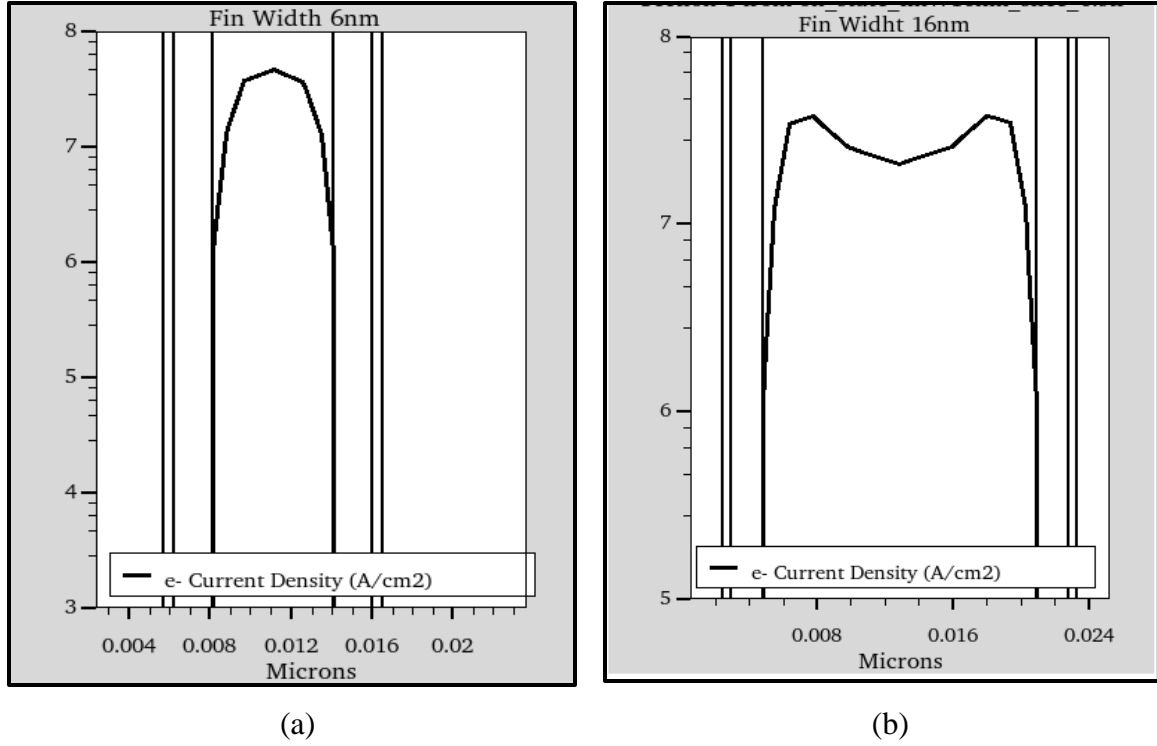


Figure 4.6 Electron current density profile perpendicular to channel (BB') (a) 16 nm (b) 6 nm

In Fig. 4.6 (a), we can see single volume inversion at the middle of the channel. However, 16nm fin thickness electron density profile (Fig. 4.5 (b)) shows two inversion layers at the side walls. Comparing electron densities for fin thickness of 6nm and 16 nm, it can be concluded that 16 nm of fin thickness provides smallest inversion thickness. The inversion layer is formed away from Si/SiO₂ interface which increases effective oxide thickness results in threshold voltage enhancement.

Chapter 5

Device Design for Optimum Performance

In this chapter, the impact of punch-through stop doping, source/drain extension engineering, and gate workfunction on the OFF-state current and transconductance are investigated and results are discussed below.

5.1 Effect of Punch-through Stop Implant (PTS)

It is well known that threshold voltage of an n-type (or p-type) metal oxide field effect transistor (MOSFET) can be increased by increasing p-type (n-type) doping in the channel. However, higher doping in channel results severe mobility degradation which in turn degrades transconduction and transit frequency. In FinFET, PTS implants (angle implant) are carried out below the fin where the gate control becomes weak as shown in Fig. 5.1 in order to control SCEs.

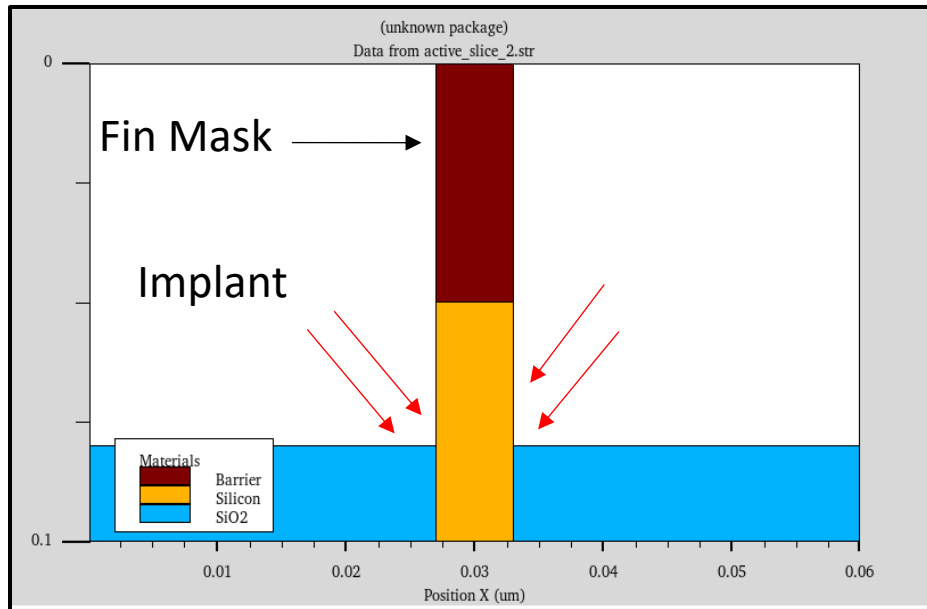


Figure 5.1 Fin cross section showing angle implant for punch through stop layer.

The threshold voltage is changed by changing the dose of punch-through stop (PTS) implant wherein the peak of the implant is located below the fin. Due to the tail of PTS implantation, the channel region does not remain completely undoped.

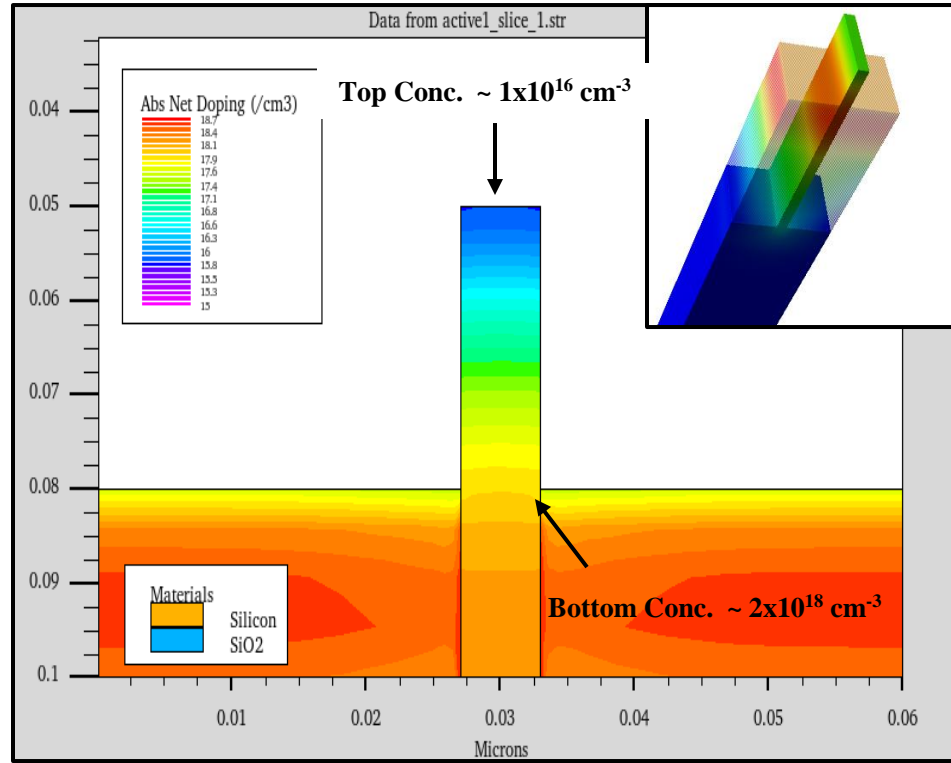


Figure 5.2 Fin cross section after punch through stop implant. Inset 3D FinFET structure showing doping concentration at the top and bottom of fin

Fig. 5.2 shows doping concentration at the top and bottom of the fin after angle implant. To evaluate leakage performance, we sweep the p-type PTS doping from 1×10^{17} - $4 \times 10^{18} \text{ cm}^{-3}$. These simulations are done for $W_F=4.6 \text{ eV}$ and $L_g=20 \text{ nm}$. Fig. 5.3 (a) and (b) shows the current-voltage characteristics for various punch-through stop doping concentration. Increasing PTS doping concentration reduces OFF state and ON state current. It is observed that OFF state current decreases exponentially with higher doping concentration however in the expense of mobility degradation as shown in Fig 5.4(a). At lower fin body doping, DIBL effect is more since the gate control below the fin is weak.

This can be observed in Fig. 5.4 where DIBL and SS decreases linearly with increasing in PTS doping concentration.

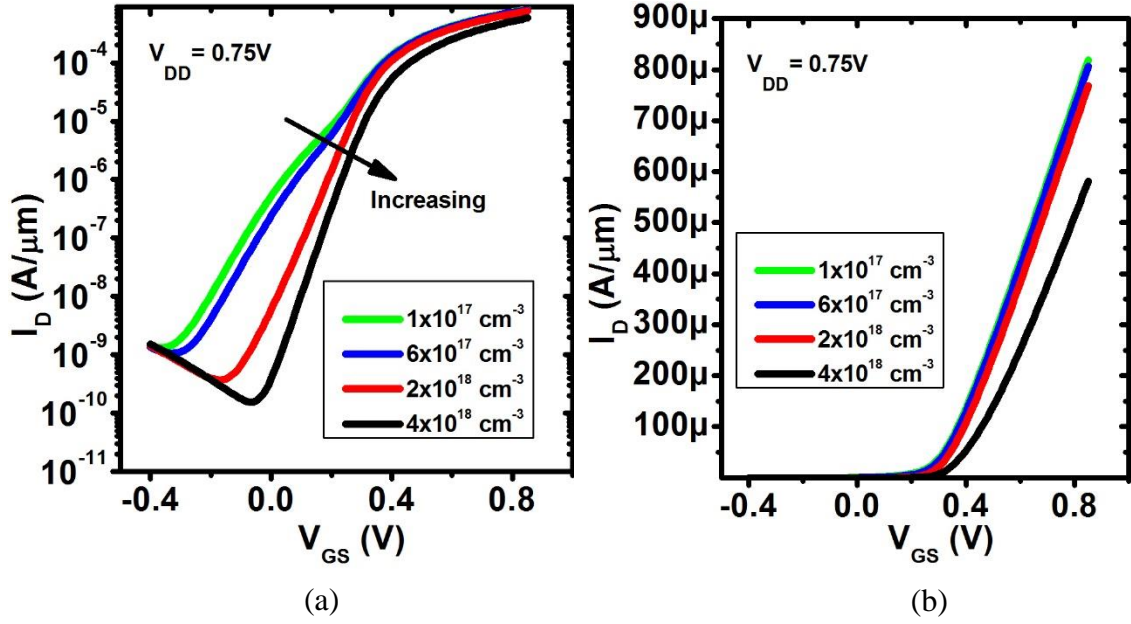


Figure 5.3 I_D - V_G comparison for different fin height (a) Linear I_D (b) Log I_D

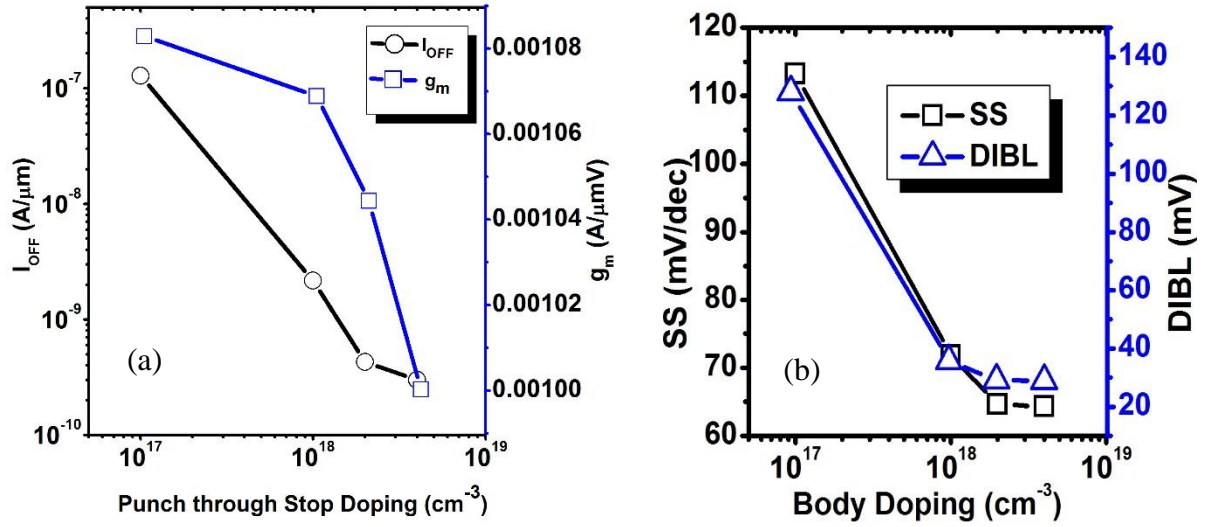
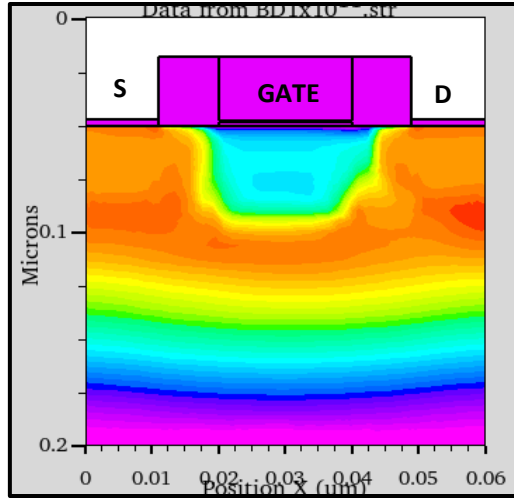
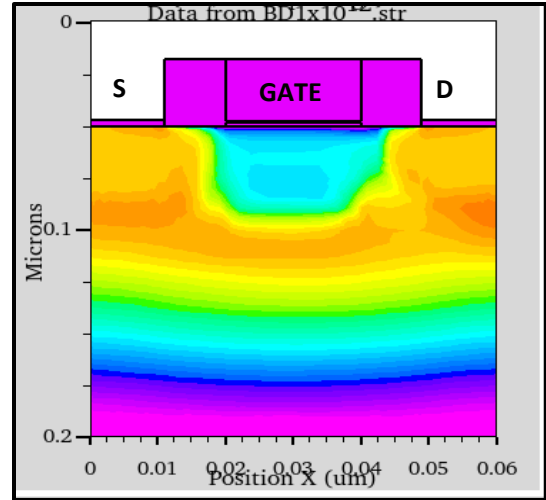


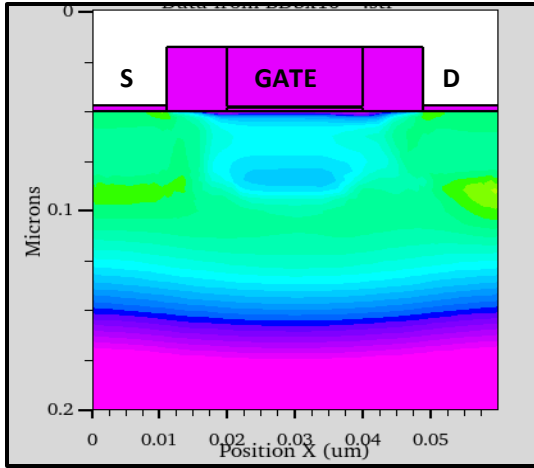
Figure 5.4 Plot showing punch-through body doping (a) I_{OFF} and g_m (b) SS and DIBL.



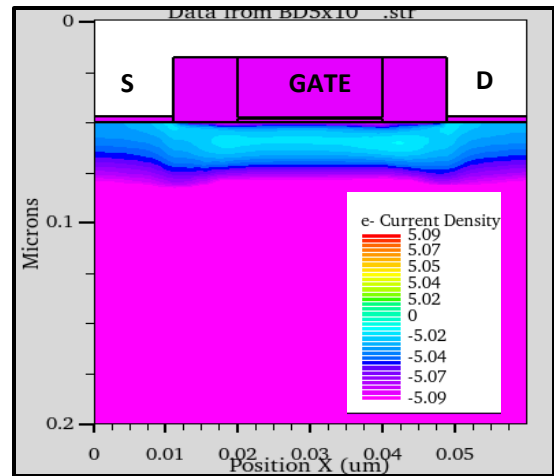
(a)



(b)



(c)



(d)

Figure 5.5 Cross section of electron current density distribution parallel to fin labeled in logarithmic scale (a) $1 \times 10^{17} \text{ cm}^{-3}$ (b) $6 \times 10^{17} \text{ cm}^{-3}$ (c) $2 \times 10^{18} \text{ cm}^{-3}$ (d) $4 \times 10^{18} \text{ cm}^{-3}$

Fig. 5.5 shows the cross section parallel to the fin showing electron current density for various doping concentration. Due to lower doping concentration below the fin, the depletion region around the drain region extends to the source side causing punch through and add to the subthreshold leakage as observed in Fig. 5.5(a). When the PTS doping is increased, the depletion width will be smaller and will not create parasitic current path. It

is clear that PTS doping tuning can help to reduce the I_{OFF} below $1\text{nA}/\mu\text{m}$ but cannot be used for ULP transistors.

5.2 Effect of Gate-Drain/Source Underlap and Overlap

The source/drain profile was modeled using the Gaussian expression

$$N(x) = N_p \exp(x^2/\sigma^2) \quad (5.2.1)$$

where N_p is the peak source/drain doping concentration and σ is the lateral straggle. The peak concentration was set to $1.5 \times 10^{20} \text{ cm}^{-3}$ and σ is varied from 1nm to 3.5nm to study the effect of source/drain gradient on gm and I_{OFF} .

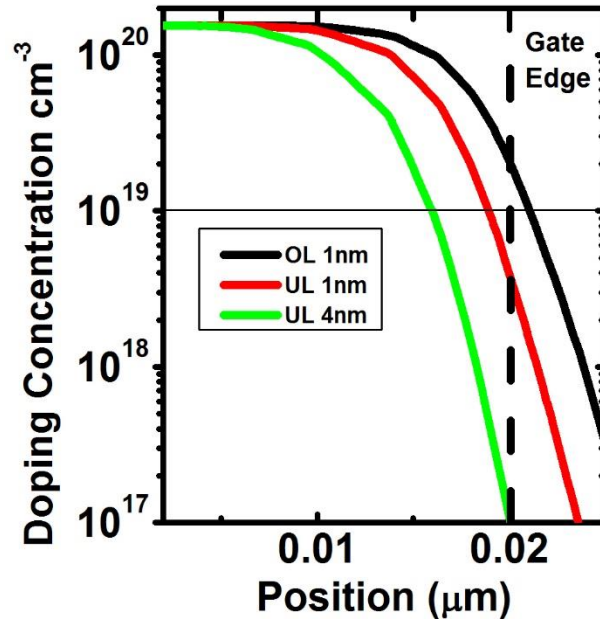


Figure 5.6 Source\Drain junction profile placement near the gate edge.

The junction underlap (UL) and overlap(OL) is defined by the position of $1 \times 10^{19} \text{ cm}^{-3}$ doping value with respect to the gate edge as shown in Fig. 5.6.

The impact of UL and OL is studied by changing the spacer thickness.

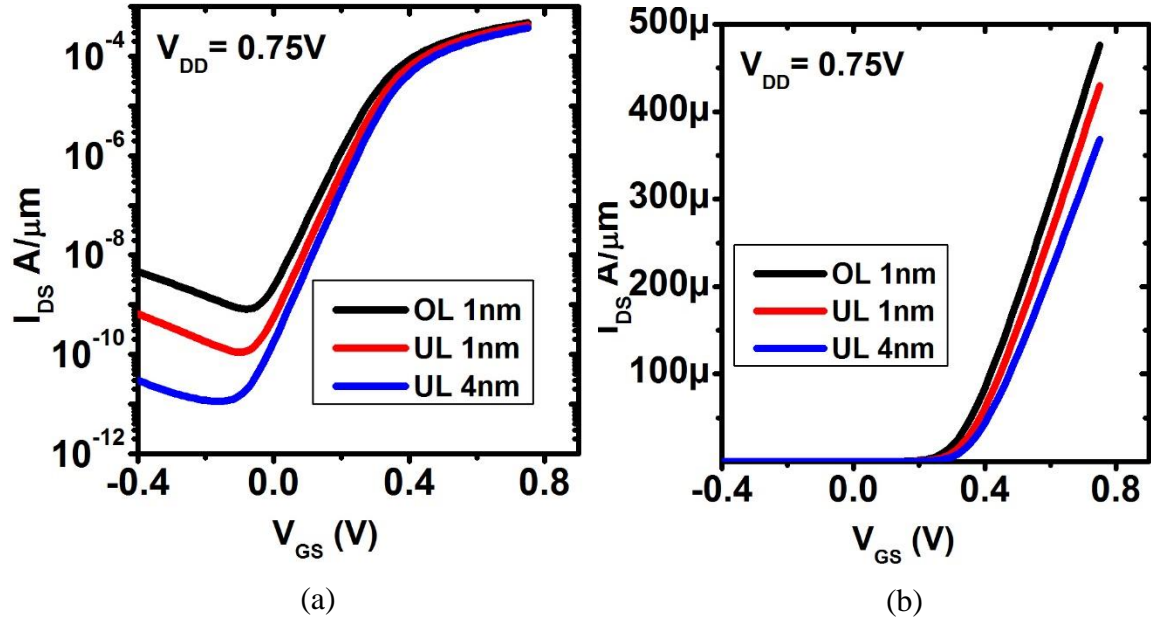
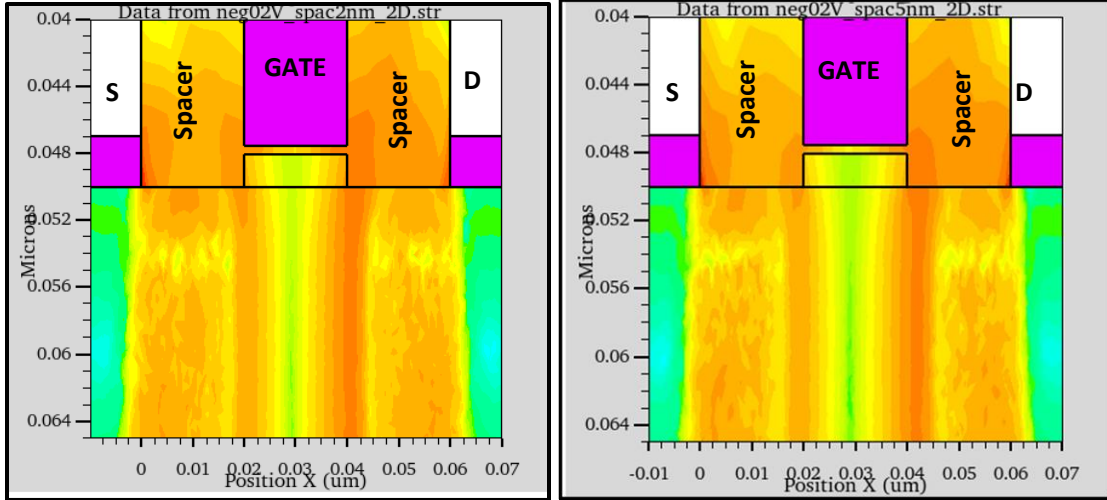


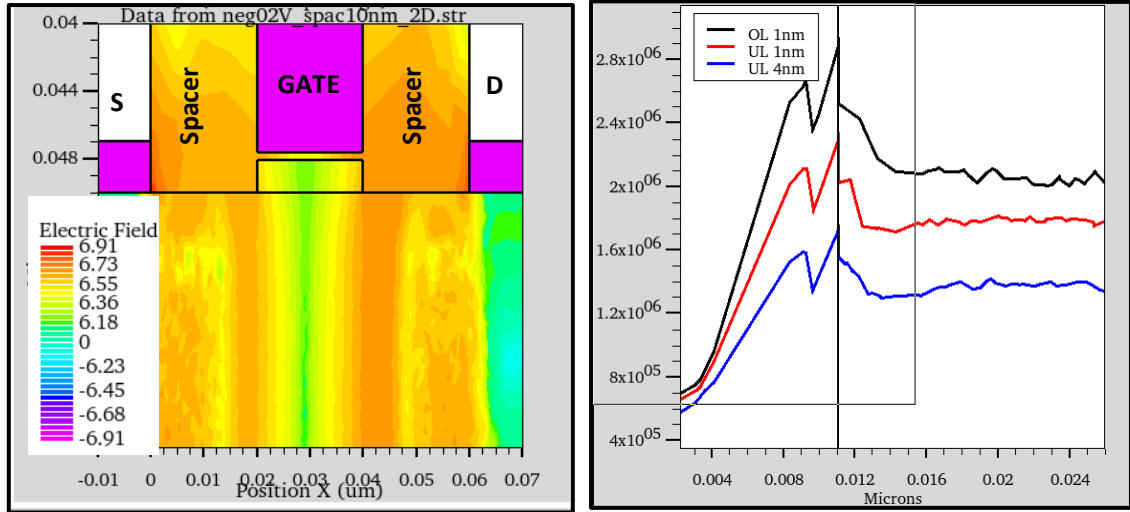
Figure 5.7 I_D - V_G characteristics showing GIDL for different junction placement (a) Log I_D (b) Linear I_D

GIDL current in FinFET depends on junction placement and gradient at shorter gate length and lower drain bias. In Fig. 5.7(a), It is observed that the GIDL current increases by two decades of magnitude for 4nm increase in junction overlap. The magnitude of GIDL depends on vertical and transverse electric field.



(a)

(b)



(c)

(d)

Figure 5.8 Electric field distribution for different junction placement labeled in logarithmic scale (a) OL=1nm (b) UL=1nm (c) UL=4nm (d) magnitude of electric field.

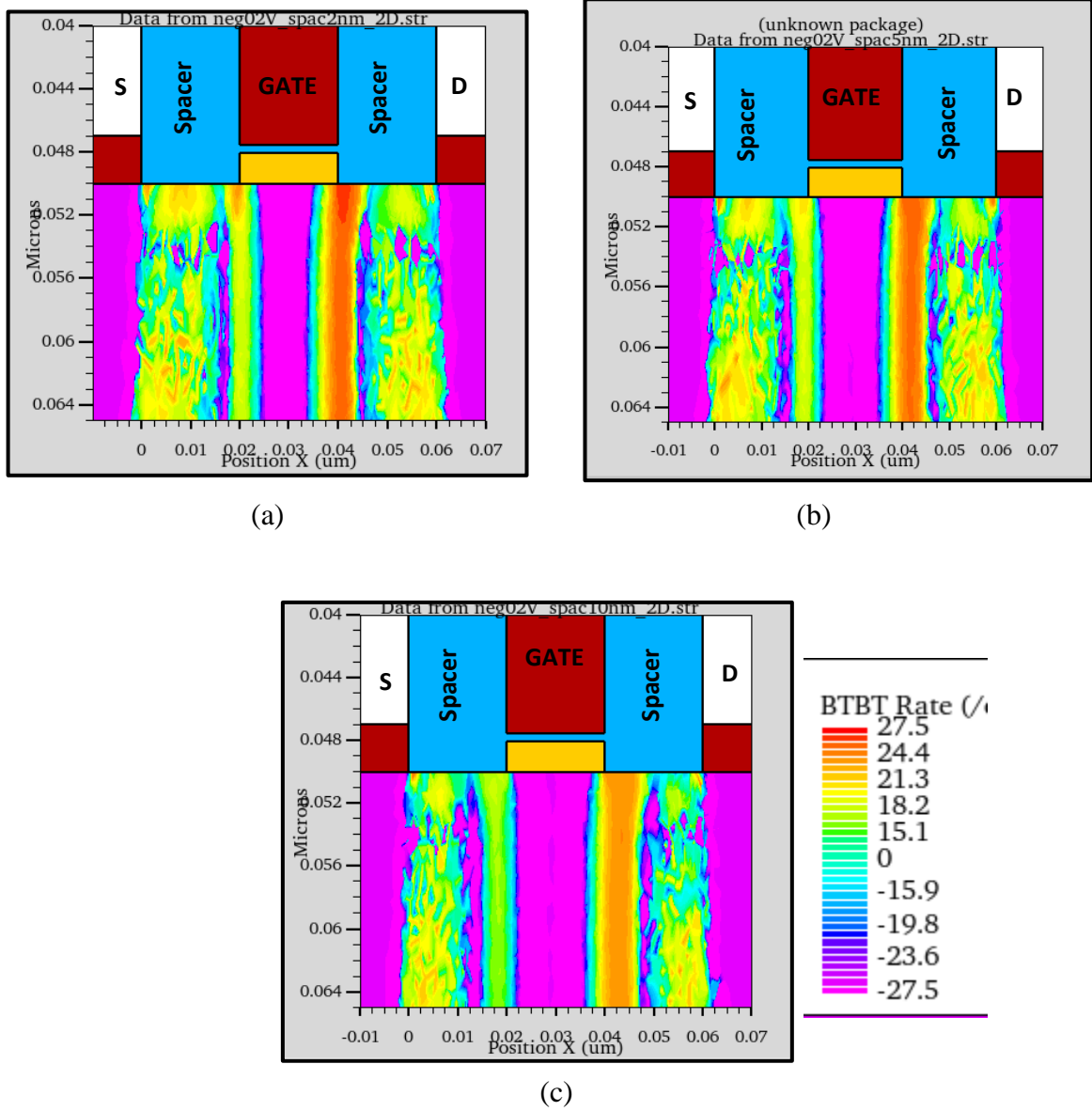


Figure 5.9 Band-to-band tunneling generation for different junction placement (a) OL=1nm (b) UL=1nm (c) UL=1nm.

Fig. 5.8 (a-c) shows electrical field for all the cases. As the junction moves away from gate, the magnitude of transverse electric field reduces (Fig. 5.8(d)) and hence BTBT generation rate is lowered as shown in Fig. 5.9 (a-c). Increasing UL leads to an increase in effective

channel length of device which results in degradation of ON current. Table 4.1 summarizes the SS, DIBL and threshold voltage for three junction placements. From the 1nm junction OL to 4nm UL, there is about 58mV of threshold voltage increase. It is observed that improvement in DIBL and SS comes at 22% reduction of ON current.

Table 4.1 Comparison between different junction profiles.

| Junction Placement | SS (mV/dec) | DIBL (mV/V) | Threshold Voltage (V) |
|--------------------|-------------|-------------|-----------------------|
| OL 1nm | 70.9 | 57.46 | 0.313 |
| UL 1nm | 67.29 | 42.8 | 0.339 |
| UL 4nm | 64.76 | 32.3 | 0.369 |

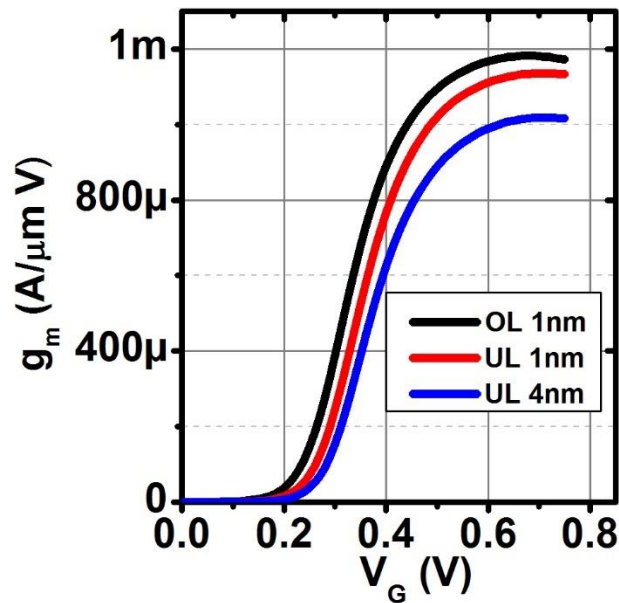


Figure 5.10 Transconductance g_m as a function of gate voltage for different junction placements.

Transconductance is also affected by moving junction away from the gate-drain region since it is inversely proportional to gate length of transistor. It can be seen in Fig. 5.10

that there is 14% decrease in g_m when there is an UL of 4nm which will reduce speed of the transistor (f_T).

5.2.1 Effect of Junction Gradient

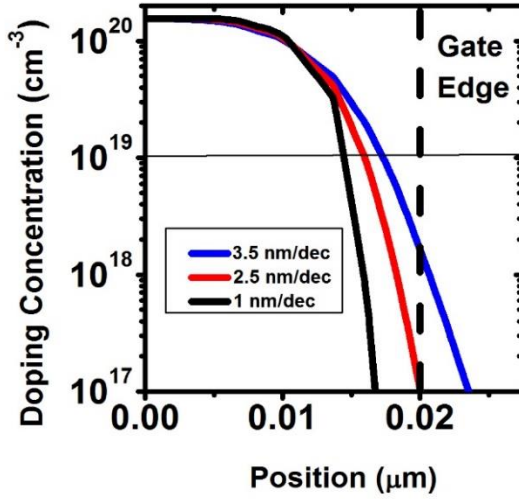


Figure 5.11 Junction gradient profile for 4nm UL cases.

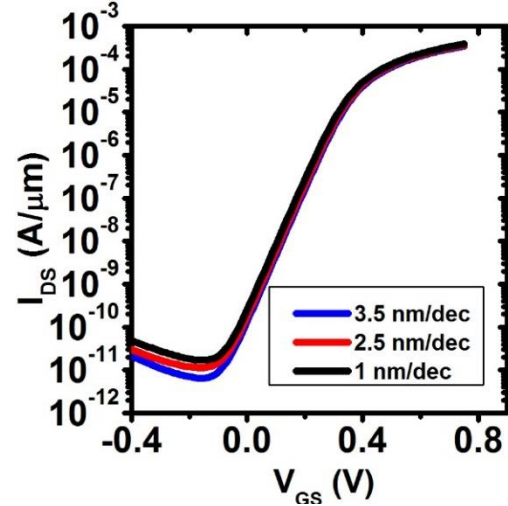


Figure 5.12 I_D - V_G characteristics showing GIDL for different junction gradient for 4nm UL.

The effect of junction gradient on OFF state current is simulated by varying lateral standard deviation for UL cases as shown in Fig. 5.11. It can be observed from Fig. 5.12 that GIDL current reduces for steeper junction profile since the effective channel length is increased and vertical junction electric field is reduced. Fig. 5.13 shows BTBT generation rate for both UL and OL cases. For the UL case, the BTBT generation rate hotspot is under the spacer region. However, in the case of OL junction, the BTBT generation hotspot is under the gate.

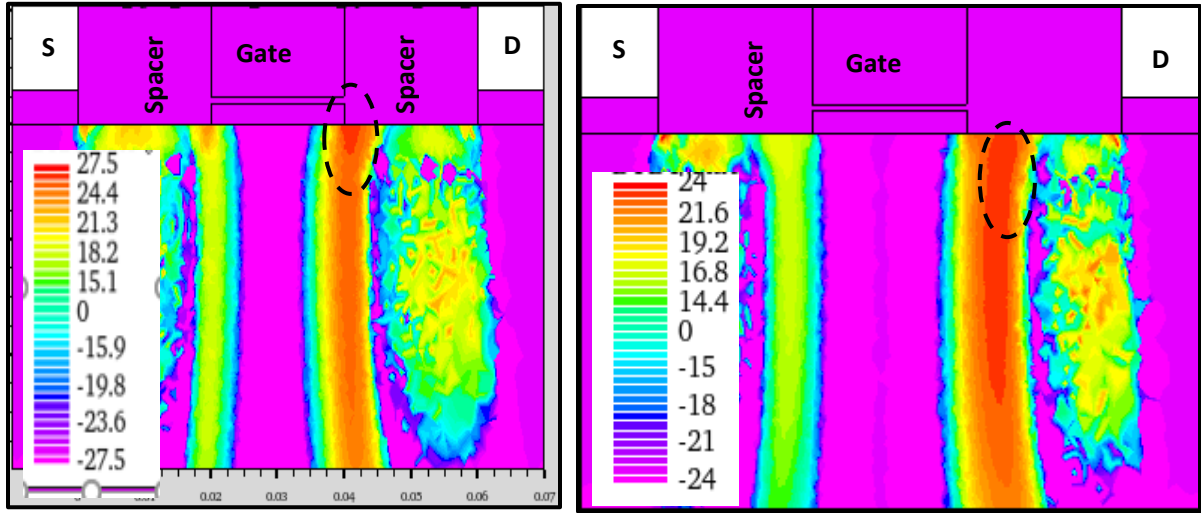


Figure 5.13 Band to band tunneling generation rate in $\text{cm}^{-3} \text{s}^{-1}$ for (a) Overlap (OL) of 1nm; (b) Underlap (UL) of 4nm.

Thus, the BTBT generation hot spot will move away from high electric field gate-drain OL region. By making steeper junction gradient.

5.3 Impact of Gate Workfunction

To control the threshold voltage of scaled MOSFET, heavy body doping is not considered as an effective way since it degrades mobility and hence the speed. The threshold voltage can be expressed as

$$V_{th} = V_{FB} + 2\Phi_f + \frac{Q_D}{C_{ox}} + V_{in} \quad (5.3.1)$$

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} = (\Phi_m - \Phi_s) - \frac{Q_{ox}}{C_{ox}} \quad (5.3.2)$$

Where, Φ_{ms} represents metal-semiconductor workfunction difference between gate electrode and the semiconductor, Φ_f is $kT/q \ln(N_a/n_i)$ fermi potential, Q_D is the depletion charge in the channel, Q_{ss} represents charge in gate dielectric, C_{ox} is the gate oxide

capacitance, and V_{in} is the additional surface potential which is required to bring inversion layer into the channel region to reach threshold point. One way to control threshold voltage is choosing appropriate gate material to tune workfunction. Over the last few year, several metal gate electrodes have been investigated as replacement over poly-Si gate such as, Mo, Ta, and $TaSi_xN_y$.

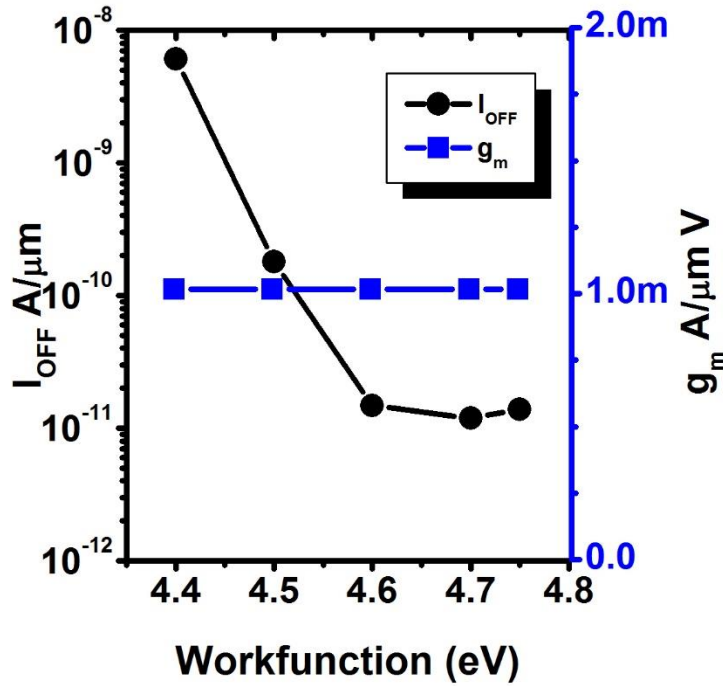


Figure 5.14 I_{OFF} and g_m as a function of gate metal workfunction.

Here the metal gate WF is varied from 4.40eV-4.75eV. The PTS doping concentration used is $2 \times 10^{18} \text{ cm}^{-3}$ with gate-source/drain UL of 4nm. Fig. 5.14 shows the impact of WF on I_{OFF} and g_m . It can be observed that the magnitude of OFF-state current decreases with increase in WF. Since, the flat-band voltage which a difference between workfunction of gate electrode and channel is a function of threshold voltage. Thus, increasing gate WF results in enhancement of threshold voltage. Beyond 4.6eV, the GIDL current dominates

and I_{OFF} is slightly increased for 4.7eV. However, transconductance remains unchanged. Therefore, by changing the gate WF, OFF current $<10\text{pA}/\mu\text{m}$ can be achieved.

5.4 Benchmarking

In this section, we compare the I_{OFF} and transit frequency of the transistors for all the three cases discussed above. Transit or cut off frequency of transistor is defined as the frequency where the current gain falls to zero. It is the measure of intrinsic speed of transistor. Transit frequency of transistor is given as

$$f_T = \frac{g_m}{2\pi C_{gs}} \quad (5.4.1)$$

Where g_m is transconductance and C_{gs} is gate to source capacitance. At saturation

$$C_{gs} = \left(\frac{2}{3}\right) L_G C_{ox} \quad \text{F}/\mu\text{m} \quad (5.4.2)$$

Fig. 5.15 shows a plot of I_{OFF} versus intrinsic frequency, f_T . For LP and ULP applications we would like to achieve highest intrinsic frequency at the lowest value of the OFF current. It can be observed that even though WF does not affect peak value of g_m , it is not enough to meet the I_{OFF} target for the ULP applications. Increasing the doping concentration results in decrease in I_{OFF} due to increase in V_T in addition to decrease in the intrinsic speed. For ULP application, a transistor with a gate length of 20nm with body doping concentration of $2 \times 10^{18} \text{ cm}^{-2}$ and UL of 4nm with WF of 4.6eV can achieve $I_{OFF} \sim 10\text{pA}/\mu\text{m}$ at 0.75V.

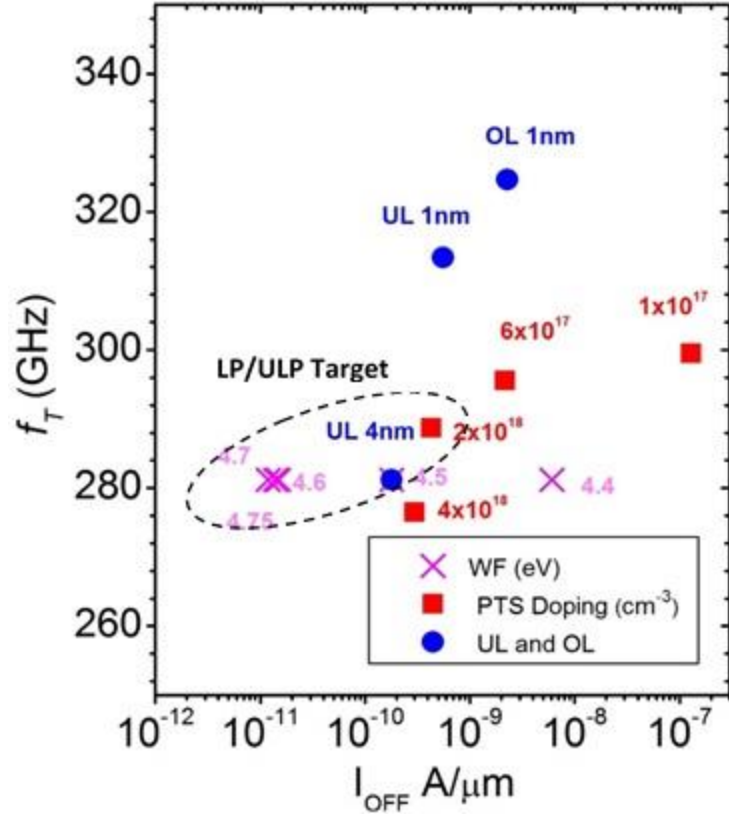


Figure 5.15 Cut-off frequency, f_T versus off state current, I_{OFF} graph showing the impact of fin body doping, gate workfunction and source-drain extension engineering on off state current and cut off frequency.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this study, the effect of fin geometry on subthreshold characteristics have been investigated and compared various threshold voltage techniques to meet low and ultra-low power requirement using 3D process and device simulation. For this purpose, a new optimized method has been proposed to significantly reduce leakage current. A basic theory of FinFET technology, its operating principle and the limitation over planar MOSFETs was also studied.

In FinFET, the 3D structure that rises above the gate called “Fin” is wrapped by the gate providing better control on channel and allowing very less current leak through body in subthreshold regime. The fins form the source/drain region, effectively providing more volume than planar MOSFETs. Fin shape has significant impact on transistor leakage and drive current. Taller fin provides improvement in drive current due to increase in effective fin width. In order to reduce the effect of drain electric field into the channel, the fin thickness is made less than 3 to 4 times the gate length of transistor. Also, thinner fins provide better gate electrostatics and improves DILB and SS. However, due to quantum confinement of carriers in thinner fins, the inversion layer thickness (T_{inv}) increase which causes enhancement in the threshold.

To meet the OFF state current requirement for LP and ULP devices, various threshold voltage techniques have been investigated. First, the punch-through stop doping is varied to see its impact on leakage current and transconductance. It was found that higher

PTS doping suppresses the SCEs but reduces g_m due to mobility degradation. Second, using source/drain junction engineering, the leakage current mainly due to GIDL was reduced. For this purpose, the spacer thickness is varied to study gate-drain/gate-source OL and UL effect on OFF state current and g_m . Results show that, OL of 1nm increases GIDL current whereas UL of 4nm suppresses GIDL current by two orders of magnitude. In third, we have investigated the effect of gate workfunction to modify threshold voltage. It was observed that, the transconductance is not affected by gate workfunction. Also, the OFF current can be reduced below 50pA/ μm . In the benchmarking plot, transit frequency f_T versus OFF current is compared for all the three cases that were discussed. It was found that the gate length of 20nm can meet requirements of the LP and ULP transistors by optimal choice of the gate work function, source drain extension engineering and PTS doping concentration in the Fin.

6.2 Future Work

This work was aimed at simulation of bulk Si bulk FinFET with rectangular fin. For the future work, important suggestions are as follows

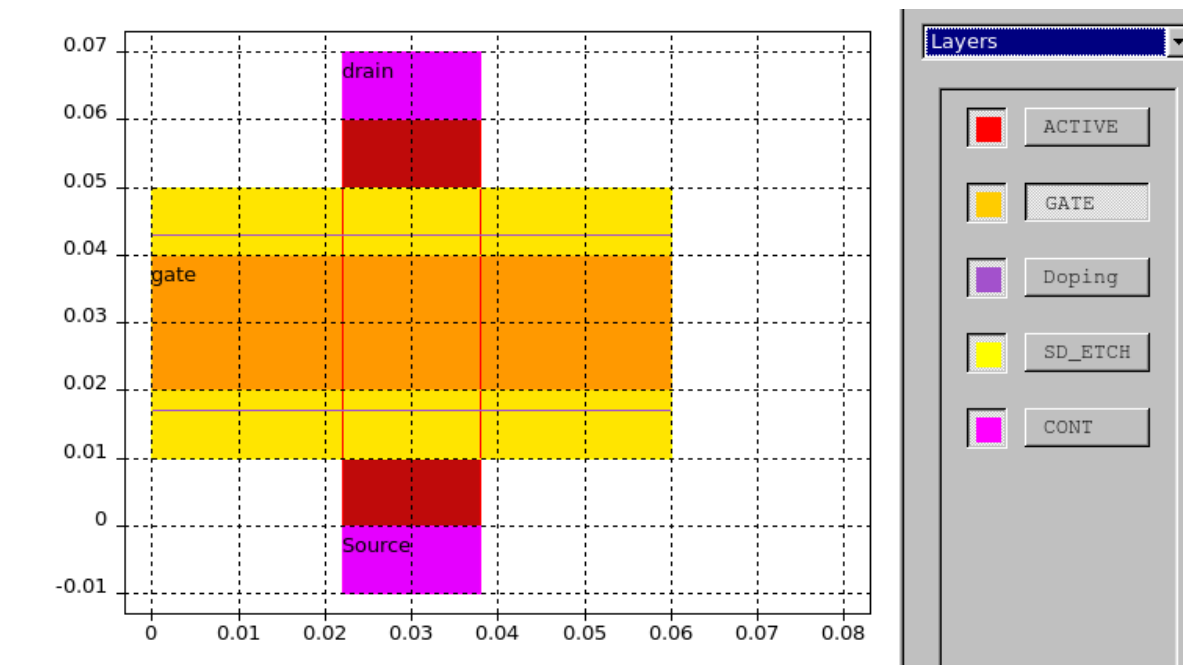
- ❖ As silicon CMOS reaching its scaling limits alternate material such as Ge or III-V semiconductor can provide higher carrier velocity.
- ❖ Strain engineering using SiGe (or SiC) raised source/drain (RSD) for PMOS (NMOS), to improve FinFET performance.
- ❖ Fully Depleted Silicon on Insulator (FD-SOI) or Gate-all-around (GAA) can also be viable alternative to FinFET for IoT applications.
- ❖ 2D (two-dimensional) material such as MoS₂ can be perfect channel material for FETs and will become successor of conventional semiconductor.

Appendix A: Mask Layout

The mask layout shown in figure below is created by using “SPECIFYMASKPOLY” statement which can be used to create new mask layer consisting of single polygon or add another polygon layer to the existing one e.g. the “Active” mask is created using following command

```
SPECIFYMASKPOLY MASK="ACTIVE" P1="0.027,-0.01" P2="0.027,0.07"  
P3="0.033,0.07." P4="0.033,-0.01"
```

Then this mask layout is used to pattern different layers e.g. An ‘Active’ layer (Red colored) defines the silicon fin. The thickness of fin is varied by changing the width of ‘Active’ layer.



Appendix B: Silvaco input files

A.1 Victroyprocess input file

```
go victoryprocess simflags="-P 4"

Init material=silicon from="0,-0.01" to="$dom_x,$dom_y" \ depth=$Sub_H gasheight=1

dopant=boron dopingvalue=1e12

#option doping.off

option print.zlines


## create active mask

## Fin thickness 6nm #####

specifymaskpoly maskname="ACTIVE" P="0.027,-0.01" \ P="0.027,0.07"

P="0.033,0.07" P="0.033,-0.01"


# create Gate mask mask with electrodes

specifymaskpoly maskname="GATE" P="0,0.02" P="0,0.04" \ P="0.06,0.04"

P="0.06,0.02" electrode=gate


## Create S/D mask with electrodes

specifymaskpoly maskname="Doping" P="0,0.019" P="0,0.041" \ P="0.06,0.041"

P="0.06,0.019" ## Spacer ##

specifymaskpoly maskname="SD_ETCH" P="0,0.01" P="0,0.05" P="0.06,0.05"

P="0.06,0.01"

#### Top Cont ####
```

specifymaskpoly maskname="CONT" P="0.027,0.06" P="0.027,0.07" P="0.033,0.07"

P="0.033,0.06" electrode=drain add

specifymaskpoly maskname="CONT" P="0.027,-0.01" P="0.027,0.0" P="0.033,0.0"

P="0.033,-0.01" electrode=Source add

Masks.lay should be saved to your directory

save name="mask"

cartesian mask="ACTIVE" spacing=0.0005 all.point ondomain

cartesian mask="GATE" spacing=0.0008 all.point ondomain

cartesian mask="SD_ETCH" spacing=0.0008 all.point ondomain

cartesian mask="CONT" spacing=0.0025 all.point ondomain

line z location=-1 spacing=0.1

line z location=-0.01 spacing=0.0005

line z location=0 spacing=0.0005

line z location=0.025 spacing=0.0005

line z location=0.05 spacing=0.0005

line z location=0.075 spacing=0.005

line z location=0.1 spacing=0.006

line z location=0.3 spacing=0.025

line z location=0.5 spacing=0.1

set cha_doping=5e12

etch silicon thick=0.05 max

implant boron energy=2 dose=\$cha_doping tilt=0 rotation=0

etch silicon angle=90 thickness=0.15 mask="ACTIVE" min
 deposit oxide thick=.120 min
 mask "ACTIVE"
 implant boron energy=4 dose=1e13 tilt=7 rotation=45
 strip resist
 diffuse time=0.2 temp=1050
 deposit oxide thick=.03 min
 mask "Doping"
 ## Source/Drain doping ##
 DOPING ARSENIC DOSE=5e14 PEAK=0.01 \
 SIGMA=0.013 LATERAL=0.0025
 strip resist
 etch oxide thick=0.04 min
 deposit material=hfo2 thick=0.0019 conformal
 mask "GATE"
 etch material=hfo2 max
 strip material=barrier
 deposit oxide thick=0.0005 conformal
 deposit polysilicon thick=0.03 max
 etch polysilicon mask="GATE" thick=0.1 max
 deposit oxide thick=0.01 conformal
 etch oxide thick=0.01 max
 etch oxide mask="SD_ETCH" thick=0.05 max

```

mask "CONT" reverse

deposit polysilicon thick=0.003 min dopant=boron dopingvalue=1e18

strip material=barrier

export victory(delaunay) structure="lg20_OL1nm_grad25.str" max.size=0.005 \
    max.interface.size=0.0008 max.interface.distance=0.04 \
    max.junction.size=0.0008 max.junction.distance=0.04

quit

```

A.2 VictoryDevice command file

```

go victorydevice simflags="-P 8"

mesh infile=lg20_delmesh_25nmdec_5nm_ch55e12.str

electrode name=gate region=3

electrode name=drain region=4

electrode name=source region=5

electrode name=substrate back

contact name=gate workfunc=4.5

models cvt consrh auger

models bbt.a=3.29e15 bbt.b=23.8e6 bbt.gamma=2.5 print

model bqp.n bqp.ngamma=1.4 bqp.nalpha=0.3

method pam.gmres maxtrap=6 itlimit=150 dvmax=1.0 carr=2 norm.scaling.local

```



```

solve init bqp.sc

solve prev

solve vdrain=0.001

solve vdrain=0.01

solve vdrain=0.05

#solve vstep=0.01 vfinal=0.75 name=drain previous

log outfile=lg20_delmesh_25nmdec_5nm_ch55e12_LD.log

Solve vgate=-0.4 vstep=0.01 vfinal=-0.2 name=gate

output con.band

output u.bbt

output val.band

output recomb u.srh

output u.trap

#Save outf=02V_lg20_spac10_bd1e12_ch5e10.str

Solve vgate=-0.19 vstep=0.01 vfinal=0 name=gate

output con.band

output u.bbt

output val.band

output recomb u.srh

output u.trap

#Save outf=0V_lg20_spac10_bd1e12_ch5e10.str

```

```
Solve vgate=0.01 vstep=0.01 vfinal=0.75 name=gate

OUTPUT E.MOBILITY

output con.band

output u.bbt

output val.band

output recomb u.srh

#Save outf=on_state_lg20_spac10_bd1e12_ch5e10.str

#Solve vgate=0.76 vstep=0.01 vfinal=0.95 name=gate

log off
```

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